Dynamic Modeling of AI Data Center Load in PSCAD

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Open-Source Model Link

Large Load Modeling

Suggested Citation

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Summary

The rapid growth of AI data centers has introduced increasingly large and highly dynamic power-electronic loads, posing significant challenges to power system operation and stability. This report presents an open-source electromagnetic transient (EMT) model of a double-conversion uninterruptible power supply (UPS)-based AI data center developed in PSCAD. The model is developed based on the publicly available information and has not been validated against actual hardware, and does not intend to represent any specific data center design. The intent of this model is to provide a conceptual model that captures the phenomena, like ride-through, to understand the origin of these behaviors and develop a basic understanding of mitigation solutions. The model adopts a modular, bottom-up design approach and captures detailed representations of key components, including the rectifier, inverter, bidirectional DC/DC converter, battery energy storage system, variable-frequency drive (VFD) cooling load, and aggregated computing loads. Both switching and average models of the power converters are implemented, with results showing that the average model substantially improves simulation efficiency while preserving the essential low-frequency dynamics. In addition, a centralized voltage and frequency ride-through module is developed to capture UPS protection logic, operating mode transitions, and tripping and reconnection behavior.

The model supports multiple operating mode configurations, including bypass mode, normal converter mode, and battery backup mode, and incorporates realistic operating scenarios such as voltage sag events, fast and slow reconnection strategies, and time-varying computing load profiles. Simulation results validate the capability of the proposed model to accurately represent UPS dynamics and capture critical interactions between large AI data center loads and the power grid.

Table of Contents

Abbreviations

AI	Artificial Intelligence
AC	Alternating Current
CPU	Central Processing Unit
DC	Direct Current
d-axis	Direct Axis
EMT	Electromagnetic Transient
FOC	Field-Oriented Control
FRT	Frequency Ride Through
GFL	Grid Following
GFM	Grid Forming
GPU	Graphics Processing Unit
HCC	Hysteresis Current Control
HV	High Voltage
HVRT	High Voltage Ride Through
IGBT	Insulated-Gate Bipolar Transistor
IT	Information Technology
LC Filter	Inductor-Capacitor Filter
LV	Low Voltage
LVRT	Low-Voltage Ride Through
MV	Medium Voltage
PCC	Point of Common Coupling
PDU	Power Distribution Unit
PFC	Power Factor Correction
PI	Proportional-Integral
PLL	Phase-Locked Loop
PSCAD	Power Systems Computer-Aided Design
pu	Per Unit
PUE	Power Usage Effectiveness
PWM	Pulse-Width Modulation
q-axis	Quadrature-Axis
RMS	Root Mean Square
SOC	State of Charge
SPWM	Sinusoidal Pulse Width Modulation
UPS	Uninterruptible Power Supply
VFD	Variable-Frequency Drive
VRT	Voltage Ride Through
VSC	Voltage-Source Converter

1. Introduction

An artificial intelligence (AI) data center is a facility that houses the specialized information technology (IT) infrastructure required to train, deploy, and deliver AI applications and services. It includes advanced computing, networking, and storage architectures, as well as the power and cooling capabilities to support large-scale AI workloads [1]. From the electrical infrastructure perspective, an AI data center can be viewed as a tightly coupled system comprising grid interconnection equipment, power converters, energy storage, computing loads, and cooling loads. Various design architectures are available for AI data centers, and one typical example is shown in Figure 1 [2].

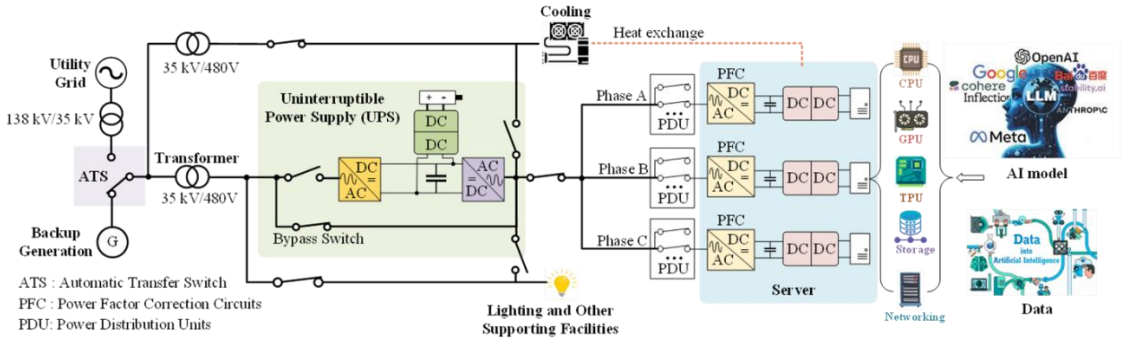


Figure 1: Typical AI data center electrical architecture based on a double-conversion UPS system.

Based on publicly available information [3], [4], this work develops an open-source electromagnetic transient (EMT) dynamic model of the electrical infrastructure of an AI data center in the software Power Systems Computer-Aided Design (PSCAD) [5]. The model is built upon a double-conversion uninterruptible power supply (UPS) system architecture and is shown in Figure 2. Specifically, the PSCAD model includes:

- The UPS system, comprising the rectifier, inverter, battery, and bidirectional DC/DC converter.
- The cooling load, modeled as a variable-frequency drive (VFD) motor.
- Aggregated AC/DC computing loads.
- Multiple operating modes (including bypass mode, normal converter mode, and battery backup mode), along with voltage/frequency ride-through and protection control modules.

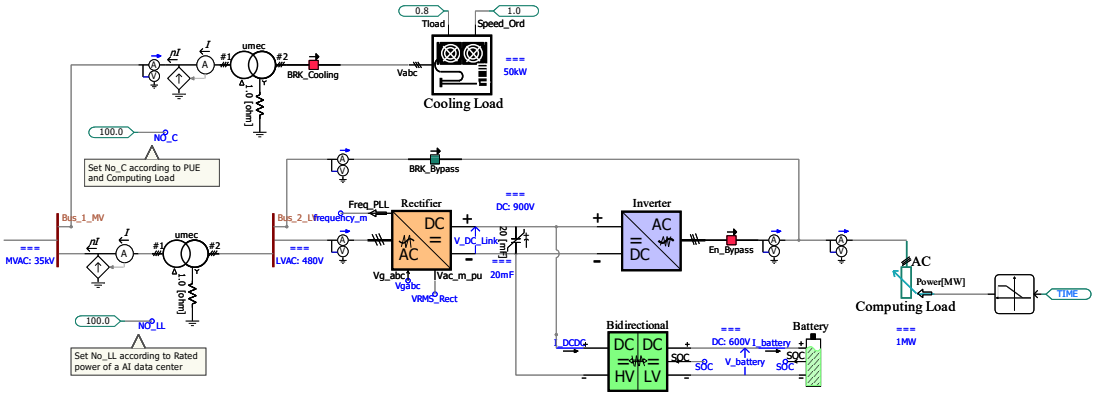


Figure 2: The open-source PSCAD model of a double-conversion UPS-based AI data center.

This open-source model is developed using a bottom-up, modular approach, and a library of key component modules is provided to support flexible adaptation. In addition, the model is scalable in power capacity and represented in per unit (pu), with the electrical parameters automatically computed based on the predefined power capacity. The model provides a detailed reference for dynamic modeling of large data center loads, which can be used for grid interaction and dynamic impact studies, such as disturbance ride-through behavior, post-fault recovery, grid control interaction, sub-synchronous oscillations, and system stability.

The remainder of this report is organized as follows. Section 2 provides an overview of the open-source model and its key parameter settings. Section 3 introduces the model library, main circuits, switching models, and control methods of the power converters. Section 4 presents the average models of power converters, in which high-frequency switching dynamics are eliminated. Section 5 introduces a centralized UPS voltage and frequency ride-through module for coordinated control of the rectifier, inverter, and DC/DC converter. Section 6 presents the double-conversion UPS-based AI data center model, along with test cases demonstrating voltage ride-through performance, operating mode transitions, and computing load fluctuations. Finally, Section 7 concludes this report and outlines future work.

2. Overview of the Open-Source AI Data Center Model

This open-source model is developed to study the electromagnetic transient behavior of large-scale AI data centers and assess their interactions with electric power grids. A high-fidelity AI data center dynamic model has been implemented in PSCAD and made publicly available to support research and engineering studies in this area. The model includes several commonly used power electronic converters in data centers, with both detailed **switching models** and computationally efficient **average models** provided. The switching models are suitable for capturing high-frequency transient and converter-level behaviors, while the average models are recommended for studies focused on lower-frequency dynamics or larger system-level simulations where computational efficiency is important. Building on these converter modules, the model represents a double-conversion UPS-based data center architecture that reflects a common practical configuration in modern AI data centers. With this framework, users can analyze the dynamic behavior of an individual data center in detail or integrate multiple data center models into a power system to study their collective grid impacts.

Moreover, the model provides a centralized UPS control module for voltage ride-through (VRT) and frequency ride-through (FRT) during mode transitions. This control module is designed to simulate how the data center responds to grid voltage and frequency disturbances. It continuously monitors key grid signals, including voltage, current, and frequency, and compares them against predefined threshold settings. Based on the detected system conditions, the controller coordinates the operation of the rectifier, inverter, and DC/DC converter to achieve the intended ride-through response. The model also includes configurable trip and reconnection logic, allowing users to represent different protection and recovery strategies under abnormal grid conditions. This functionality is essential for studying the dynamic interactions between AI data centers and the power grid, particularly in assessing their disturbance response and grid support capabilities.

The remainder of this section first introduces the PSCAD file list for the open-source AI data center dynamic model and describes the function of each file, followed by the key parameters and their typical or default values.

2.1. Open-Source PSCAD Files

Table 1: File list and functionality of the open-source PSCAD model.

File name	File functionality
"Main_AIDataCenter_Workspace.pswx"	**PSCAD workspace.** It defines the locations of all required files. Opening this workspace automatically loads all libraries and test cases.
"AIDataCenter_Model_Library.pslx"	**PSCAD library.** It contains all models used in the test cases. This library must be added to the workspace before use. Users can copy models from the library in two ways: (1) Standard paste keeps the link to the original library; (2) Paste with transfer creates an independent module.
"TestCase_VoltageSag_Average.pscx"	**Double-conversion UPS-based AI data center test case using the average model.** It includes a 138 kV grid, 138 kV to 35 kV and 35 kV to 480 V transformers, average UPS models, computing loads, and cooling loads. Switching-level IGBT models are not included. Simulation results are shown in Section 6. This test case is recommended for low-frequency transient performance studies, such as LVRT and operational mode transitions.
"TestCase_VoltageSag_Switching.pscx"	**Double-conversion UPS-based AI data center test case using the switching model**. It provides the same functionality as "TestCase_VoltageSag_Average.pscx". Switching-level IGBT models are included in the converters.
"TestCase_ITLoadFluctuation_Average.pscx"	This case includes a variable computing load. It shows how to simulate load fluctuation based on the provided example. The file "ComputingLoad.txt" must be placed in the same folder.
"ComputingLoad.txt"	**Real GPU time-series data** from the MIT Supercloud dataset [6]. Users can modify the load profile in this file or replace it with other time-series load data as needed. The file should contain two columns: Time and GPU power.

2.2. Key Model Parameters

This section presents the key rated parameters in the model and their default values. Users can modify these parameters to reconfigure the model for different settings and study needs.

2.2.1. Grid-level Parameters

The key grid-level parameters are listed in Table 2. If only the computing load and cooling load need to be adjusted, users only need to modify the two scaling factors in the table.

Table 2: Key grid-level parameters.

Utility grid parameters	**Typical or default value**
Grid voltage	138kV
Grid frequency	60Hz
HV/MV transformer	138kV/35kV, 150MVA, Y/Delta, Leakage Reactance 0.15pu
Scaling factor of cooling load	NO_C:100 (from 50kVA to 5MVA) (Users can set this value according to the PUE and computing load capacity.)
Scaling factor of computing load	NO_LL:100 (from 1.5MVA to 150MVA).

2.2.2. Rectifier Parameters

The key parameters of the Rectifier are listed in Table 3. Among them, the parameter “Reconnection real power increase ramping limit” is critical for reconnection studies. The rectifier rated power should be set equal to or greater than the sum of the inverter rated power and the battery charging power. All per-unit rectifier parameters are defined based on the rectifier’s rated power, and careful attention needs to be paid to unit conversion.

Table 3: Key parameters of the rectifier.

Rectifier Parameters	Typical or default value
Rated power	1.5MVA (the battery charging power should be set less than the rated rectifier power minus the computing load power)
Rated AC line-to-line voltage	0.48kV
Rated frequency	60Hz
Active power order	0.7 pu (the reconnection reference power, 0.7*1.5 = 1.05MW)
DC voltage order	0.9 kV (this value should be kept consistent with the DC/DC converter)
Reconnection real power increase ramping limit	0.7 pu/s (1.05MW/s in 1.5MVA base), which means for 1MW computing load reconnection, the reconnection time is 0.95s.
Maximum rated current	1.3pu

2.2.3. Inverter Parameters

The key parameters of the inverter are listed in Table 4.

Table 4: Key parameters of the inverter.

Inverter Parameters	Typical or default value
Rated power	1MVA
Rated AC line-to-line voltage	0.48kV
Rated AC frequency	60Hz

2.2.4. DC/DC Converter Parameters

The battery charges and discharges power through a bidirectional DC/DC converter. The key parameters are listed in Table 5.

Table 5: Key parameters of the DC/DC converter.

DC/DC Converter Parameters	Typical or default value
Rated discharging power	1MW (for discharging) should equal the rated computing load power.
Charging power set-point	0.1MW (maximum value equals the rectifier rated power minus the computing load rated power.)
HV DC voltage	0.9kV (should equal or be near to the DC voltage of the rectifier)
Charging/discharging mode	0 for discharging and 1 for charging
LC DC rated voltage	0.6kV, nominal battery voltage

2.2.5. UPS DC-link Capacitor Parameter

Compared with single-phase PFC, under balanced three-phase conditions the total instantaneous power of the three phases is constant. Therefore, the DC-link capacitor in a three-phase UPS does not need to withstand the second-order (twice line-frequency) power ripple. As a result, for the same power rating, the required DC-link capacitance in a three-phase UPS is typically smaller than that in a single-phase PFC system.

The selection of the DC-link capacitor in a three-phase UPS should account for load variations, voltage fluctuations caused by three-phase unbalance, and DC voltage ripple introduced by the high-frequency switching of the DC/DC converter during battery backup mode. Due to the high switching frequency, ensuring that the DC voltage ripple meets the requirements under low-frequency load variations is generally sufficient to also accommodate the ripple induced by high-frequency DC/DC switching. The capacitance value can be determined based on the following equation[7].

$$C_{\text{DC-link}} = \frac{I_{\text{Load}}}{2\pi V_{\text{ripple}} f_{\text{dis}}}, \tag{2.1}$$

where V_{ripple} is the required maximum DC-link voltage ripple, I_{load} is the load rated current, f_{dis} is the power disturbance frequency. Here, f_{dis} may be less than the switching frequency, because the power disturbance may come from the low-frequency computing load fluctuation in AI data center.

In addition, the capacitor sizing must consider the thermal effects associated with RMS current under the dynamic operation of the rectifier, inverter, and DC/DC converter. Even under balanced three-phase conditions, although the average capacitor current is zero, significant high-frequency ripple current exists due to switching, which leads to thermal stress and must be properly accounted for. The RMS current of the DC-link capacitor is analyzed in [8].

Furthermore, some AI data center UPS systems are beginning to adopt supercapacitors to better handle computing load fluctuations and enhance low-voltage ride-through

capability. Therefore, users may select the DC-link capacitor value in simulations based on their specific UPS configurations. In the provided test case, a 1 MW UPS uses a DC-link capacitance of 20 mF. If supercapacitors are employed, a significantly larger capacitance may be selected. For more information about DC-link capacitor sizing, please refer to [9] and [10].

Finally, note that the PI control bandwidth of the DC-link voltage in both the rectifier and DC/DC converter must be properly tuned according to the chosen capacitance value; otherwise, instability may occur.

2.2.6. UPS VRT and FRT Parameters

A UPS VRT and FRT control module is included for centralized control of the rectifier, inverter, and DC/DC converter. These parameters are important for studying system ride-through behavior during a voltage disturbance. The key parameters are listed in Table 6.

Table 6: UPS VRT and FRT Protection Parameters.

UPS VRT protection Parameters	**Typical or default value**
Rated AC line-to-line voltage	0.48kV (can be 35kV if the protection is based on MV-bus measurements)
Rated frequency	60Hz
Rated capacity	1.5MVA (for rectifier current protection)
Initial mode	Bypass
Activation simulation waiting time (for initialization)	1s, to avoid unintended protection triggering due to model initialization, protection detection is enabled after 1 s.
Battery comes out delay time	1s, during the rectifier reconnection, the battery needs to keep connected with the DC link to support the load until the rectifier fully recovers. This time should equal the reconnection time (reconnection final power over the reconnection ramping rate).
Bypass switch VRT setting	Set the maximum and minimum trip voltage and maximum current, as well as the holdup time for each threshold.
Rectifier VRT enable setting	Set either that the protection is enabled or not.
Rectifier reconnection delay time	1s (once the grid voltage recovers and after this delay time, the rectifier is deblocked and starts to increase its power). **Fast or slow reconnection** is set based on this value.
LVRT/HVRT curve of rectifier	Input 10 points for the VRT curve; if some points are not used, set the holdup time to a large value.
Overcurrent protection curve	The threshold and holdup time settings for rectifier overcurrent protection.
FRT settings	Maximum/Minimum frequency threshold and holdup time for bypass breaker and rectifier. Refer to [11].

3. Switching Models of Power Converters and Computing Load

This section begins with an overview of the developed model library and a summary of the converter control strategies. It then presents the switching-level implementations of the rectifier, inverter, bidirectional DC/DC converter, and battery system. It also describes the VFD-based cooling loads and computing loads.

3.1. Model Library

The model library is illustrated in Figure 3 and comprises the modules of key electrical components in AI data centers. The converter models are categorized into two types: switching models and average models. The average models perform averaging over one pulse-width modulation (PWM) switching period, thereby eliminating high-frequency switching dynamics and significantly improving simulation speed. The switching models are presented in this section, while the average models and their comparison with the switching models are presented in Section 4.

In addition, a UPS voltage and frequency ride-through module is developed to coordinate converter operation and enable UPS mode transitions and protection functions. The computing load is modeled as a constant power load. For constant power loads, both AC-side and DC-side aggregations are implemented, allowing users to select an appropriate representation based on the modeling objective. Users can also specify load profiles to capture fluctuations in computing demand. The AC-interface computing load corresponds to the case where aggregation is performed at the three-phase AC terminals immediately after the inverter. In this configuration, aggregation is performed at the three-phase AC side, where each phase includes the power distribution unit (PDU), power factor correction (PFC), DC/DC converters, and GPU loads, yielding an equivalent three-phase AC constant load.

In contrast, if single-phase PFC circuits are present on each phase after the inverter and the aggregation is performed downstream of the PFC circuit, the load should instead be modeled as a constant power load using the DC-interface computing load.

The following subsections describe each module in detail, including its parameters, control strategy, and protection mechanisms. For the single-phase PFC circuit, readers may refer to the report on the dynamic modeling of crypto-miner loads [12]. The control design and low-frequency impedance model of the PFC are presented in [13]. Additional descriptions of the converter models and control algorithms are provided in [14]. The voltage and frequency ride-through and reconnection strategies developed in this report also account for practical considerations, including the VRT curve, reconnection delay, and ramp-rate limitations.

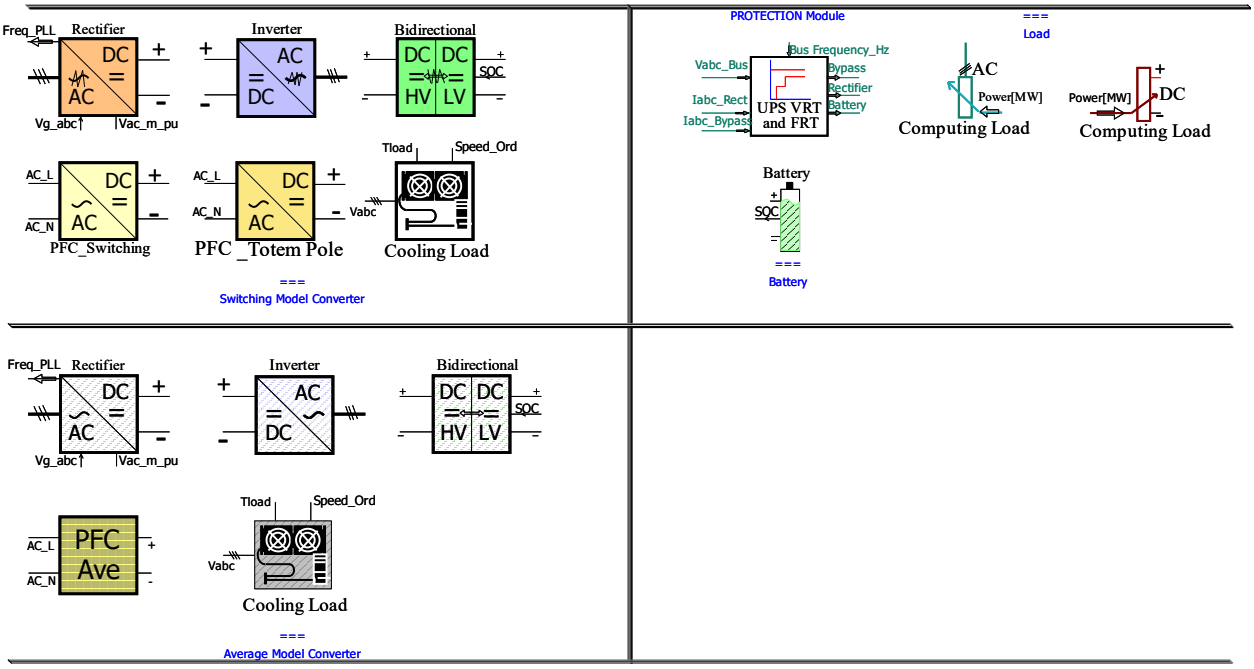


Figure 3: The PSCAD model library for AI data centers.

3.2. Power Converter Control Summary

The control methods of all power converters are summarized in Table 7:

Table 7: Summary of the control methods for all power converters in the AI data center model.

Converter Model	Circuit	Control Method		
Rectifier	Three-phase two-level voltage source converter	dq-frame decoupling double-loop (outer loop and inner current loop) control	d-axis	Active power/DC link voltage
			q-axis	Reactive power/AC voltage
Inverter	Three-phase two-level voltage source converter	dq-frame decoupling single-loop (voltage loop) three-phase voltage and frequency control	d-axis	AC voltage magnitude
			q-axis	Reference set to 0
Bidirectional DC/DC	Bidirectional DC/DC converter	Single-loop power/DC link voltage control	Buck-Mode	Power control for charging
			Boost-Mode	DC link voltage control for discharging
PFC	Power factor correction circuit (Single Phase)	Voltage and current loop control for AC to DC conversion		
Cooling Load	Variable frequency drive motor	Field-oriented control (FOC) for motor speed	d-axis	Reference set to a small value
			q-axis	Speed

3.3. Rectifier

3.3.1. Main Circuit

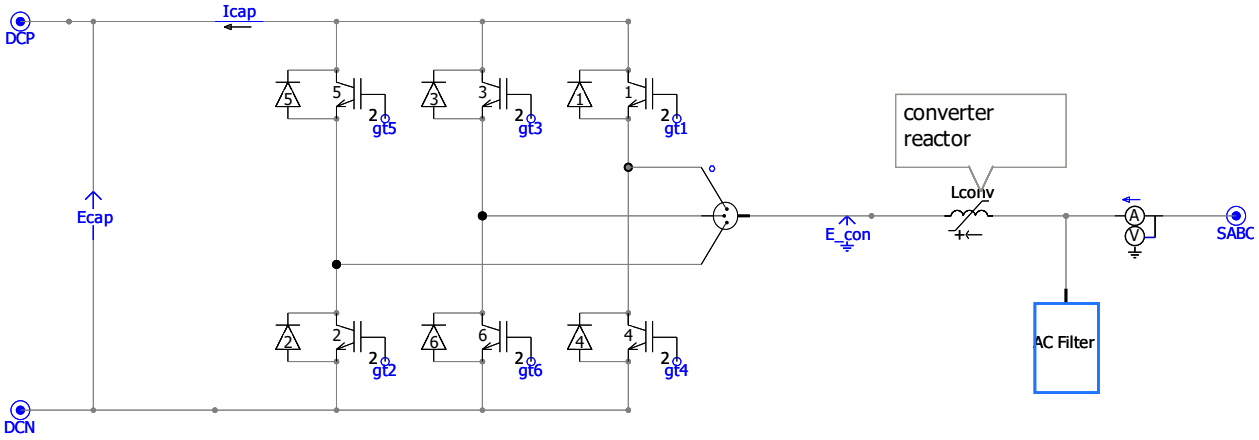


Figure 4: Main circuit of the three-phase two-level rectifier.

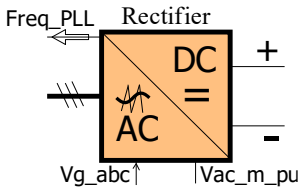


Figure 5: Rectifier graphic in PSCAD.

The grid-following (GFL) rectifier used in the model adopts a conventional three-phase, two-level voltage-source converter topology. As illustrated in Figure 4, the rectifier comprises a DC-link capacitor, a three-leg bridge, and an AC-side filter inductor. In grid-following operation, the rectifier synchronizes with the grid through a phase-locked loop (PLL). The control system regulates the AC-side currents to achieve the desired active and reactive power exchange with the grid, while the DC-link voltage is controlled indirectly through active power regulation. As a result, the rectifier behaves as a controlled current source from the grid perspective, following the grid voltage phase and frequency. As shown in Figure 5, the input signal of the rectifier includes the grid instantaneous voltage Vgabc and the measured root-mean-square (RMS) voltage VRMS_GFL. The instantaneous voltage is used for the PLL to follow the phase angle, and the RMS voltage is used for q-axis current control. The PLL measured frequency Freq_PLL is the output signal from the rectifier, which is used for UPS frequency ride-through.

3.3.2. LC Filter Parameters Calculation

In the model, the inductor-capacitor (LC) filter parameters are calculated automatically based on the rated parameters and the cutoff frequency. Two simple coefficients are used to choose the R and L parameters, as shown in Figure 6.

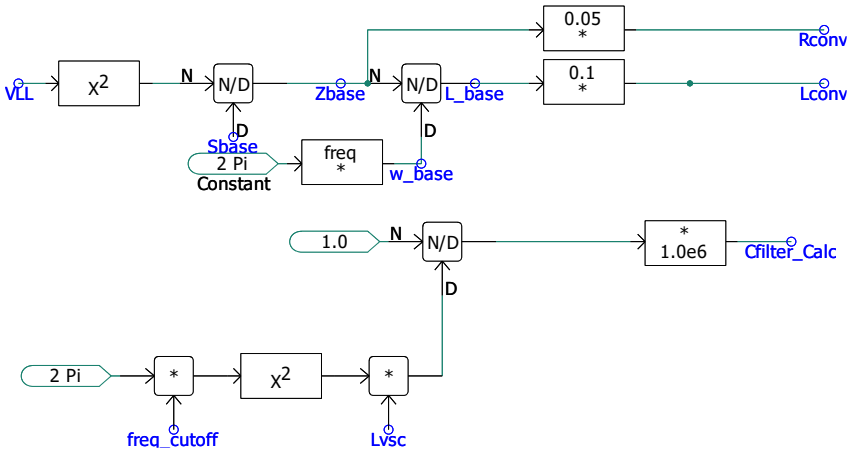


Figure 6: Rectifier LC filter parameters calculation.

The inductor and resistor values are calculated according to (3.1) and (3.2).

$$L = 0.1 \times \frac{Z_{\text{base}}}{\omega_{\text{base}}} = 0.1 \times \frac{V_{\text{LL}}{}^2}{S_{\text{base}}} \frac{1}{2\pi f_{\text{base}}}, \tag{3.1}$$

$$R = 0.05 Z_{\text{base}}, \tag{3.2}$$

where f_{base} is the AC frequency 60Hz and V_{LL} is the AC line-to-line voltage (480V is used in the model).

The impedance of the inductor is set to be 10% of the rated impedance, while the resistance is set to be 5% of the rated impedance. The capacitor value is chosen based on the cutoff frequency and the inductance value:

$$C = \frac{1}{(2\pi f_c)^2 L}, \tag{3.3}$$

where f_c is the cutoff frequency of the LC filter.

3.3.3. Control Loop

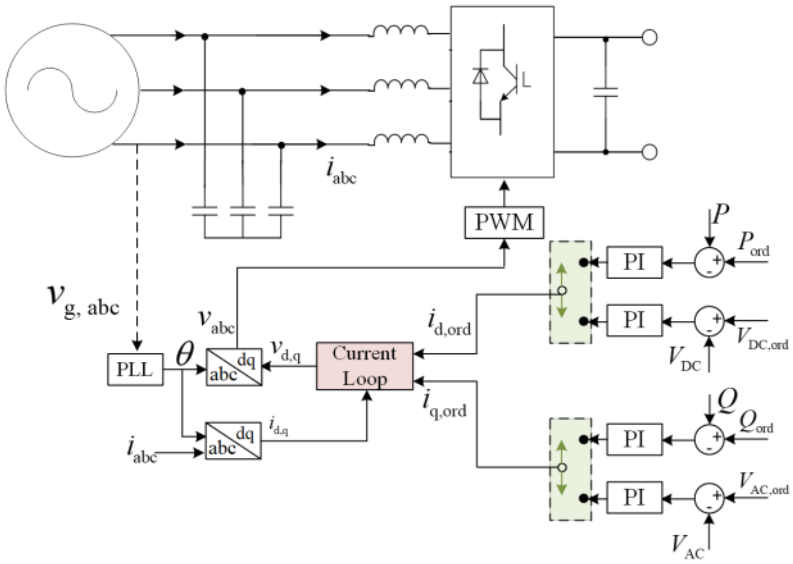


Figure 7: Rectifier d-q axis decoupling control.

The control diagram of the GFL rectifier is shown in Figure 7. The rectifier employs a conventional cascaded control architecture based on synchronous reference frame current regulation. The control system consists of a PLL, coordinate transformations, inner current control loops, and a pulse-width modulation unit. In the grid-following operation, the d-axis is aligned with the grid voltage vector, such that active and reactive power can be directly regulated through the d-axis and q-axis currents, respectively.

The inner current control loop regulates the converter output currents in the dq-frame. PI controllers are employed independently for the d-axis and q-axis current channels to track their respective current references. Feedforward decoupling terms are included to compensate for cross-coupling effects introduced by the rotating reference frame and the converter-side inductance.

3.3.3.1. d-axis Control

For the d-axis current, the control target can either be the active power or the DC link voltage, as shown in Figure 8.

When the grid voltage is normal, and the battery is not connected to the DC link, the rectifier needs to be operated in DC link voltage control mode to maintain a stable DC link voltage.

Constant AC power control is employed only when the battery is supporting the DC link (in discharging mode and controlling the DC link voltage), allowing the rectifier to provide partial power (according to the ramping rate and reference power) to the computing load. This mode is used during the reconnection. Because the reconnection ramping rate is limited to a constant value, the rectifier power is set according to this ramping rate and the final reference value. In the constant power control mode of rectifier, the battery supports the imbalanced power between rectifier and computing load and maintains the DC link voltage.

During the switching process between the two control modes, the continuity of the controller output must be considered. Therefore, when switching the d-mode (d-axis control mode), the integral term of the PI controller can be reset to match the current output of the PI controller, enabling a seamless transition.

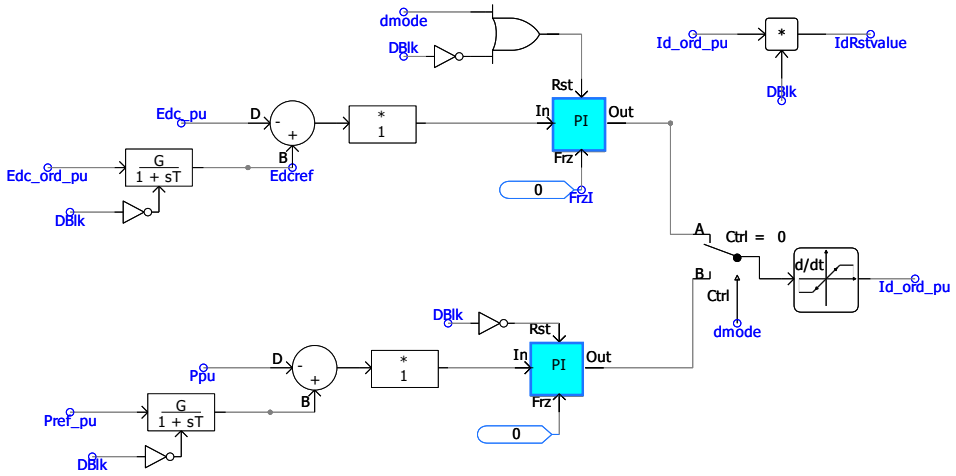


Figure 8: d-axis outer loop control.

3.3.3.2. q-axis Control

For the q-axis current control, there are also two choices: either constant reactive power Q control or AC voltage support control, as shown in Figure 9. Usually, the rectifier is

operated in reactive power Q control and set Q = 0, while AC voltage control is used only when grid voltage support is considered.

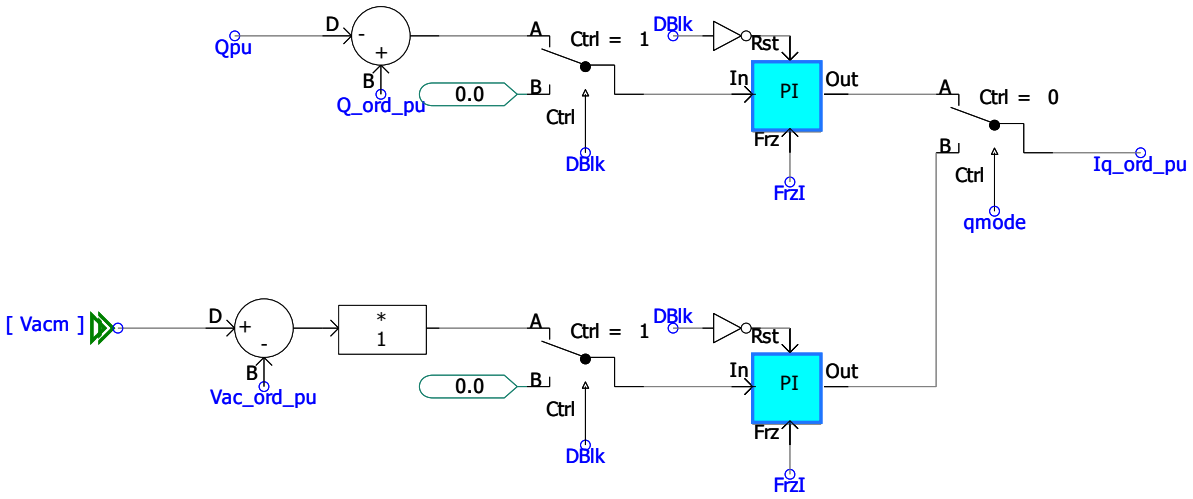


Figure 9: q-axis outer loop control.

The outputs of the current controllers generate voltage reference signals in the dq-frame, which are then transformed back to the abc-frame using the inverse coordinate transformation. These voltage references are applied to the PWM modulator, which produces the gating signals for the power semiconductor switches of the rectifier.

3.3.3.3. Current Limiter

The rectifier current is limited by limiting the input reference current id and iq, to the current loop, as shown Figure 10. When the current reaches its maximum limit, the user needs to specify the priority between the d-axis and q-axis currents. In typical operation, the rectifier's reactive power is set to zero; therefore, the d-axis current is given priority and allowed to reach the maximum value, while the q-axis current is set to zero.

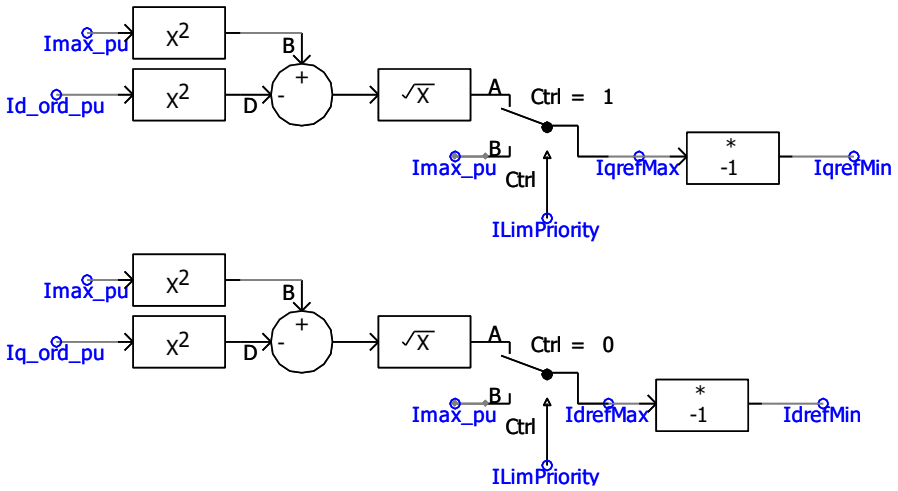


Figure 10: Rectifier current limiter.

3.3.4. Parameters

The rated parameters of the rectifier are illustrated in Figure 11, including the rated power, rated line-to-line AC voltage, and rated frequency. Based on these rated parameters, the value of the LC filter will be calculated automatically.

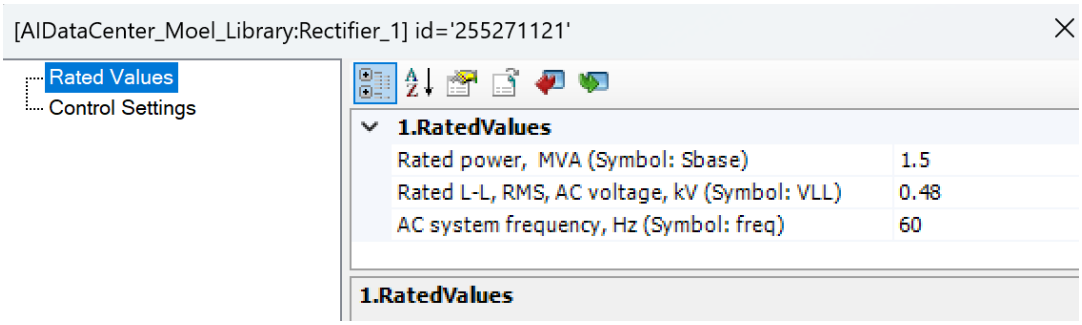


Figure 11: Rated parameters for rectifier.

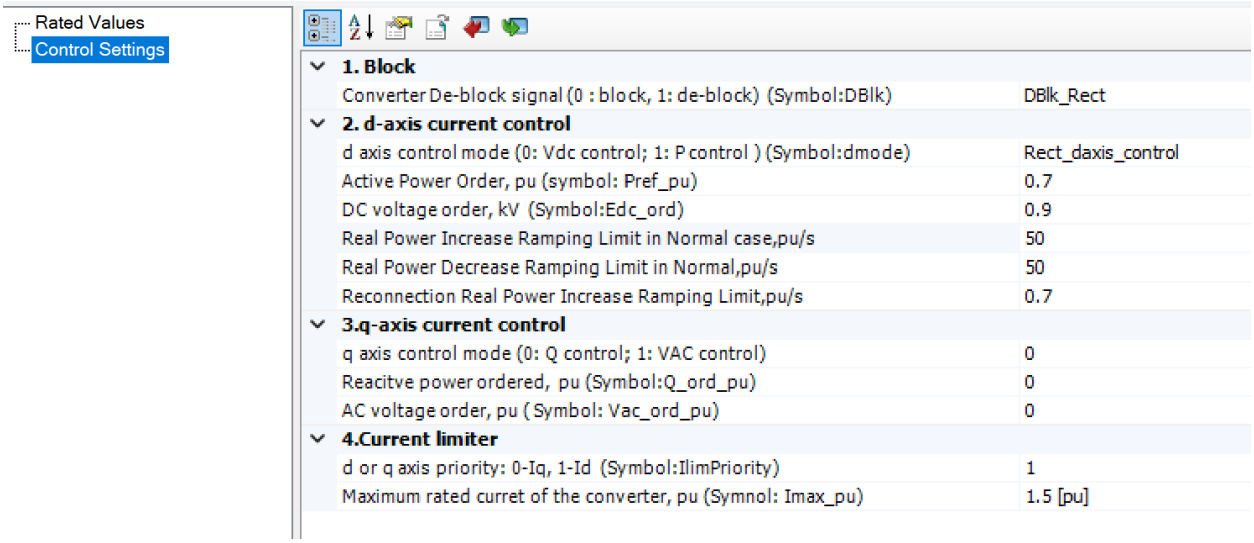


Figure 12: Control settings for rectifier.

The control settings for the rectifier are shown in Figure 12. A control signal “DBlk_Rect” is used as the block command for the rectifier (0 indicates block/disable, and 1 indicates deblock/enable).

For the d-axis current, a binary logic signal is used to select the control mode. If the d-axis is used for constant active power control, the ordered active power must be specified to be the rated computing load power. In normal operation, the d-axis current is regulated by DC-link voltage control; therefore, the ordered DC-link voltage needs to be set (typically 700 – 1000 V, which is higher than the battery voltage).

In addition, the power ramping rate can be limited under normal operating conditions. If ramp-rate limiting is not required, this parameter can be set to a large value (pu/s), e.g., 20 pu/s or 50 pu/s. After a fault and subsequent reconnection, this value is typically set to a smaller limit to restrict the power ramp rate during reconnection.

The three ramp-rate limits in the parameter set in Figure 12 correspond to constraints on the rectifier power variation during mode transitions, as illustrated in Figure 13.

During the transition from bypass mode to normal converter mode, the rectifier must rapidly take over the regulation of the DC-link voltage while minimizing disturbances to

the grid power, as the power supply is quickly transferred from the bypass switch to the rectifier. Therefore, this ramp rate should be set to a relatively large value (corresponding to the blue ramp curve in Figure 13).

When the grid voltage connected to the rectifier experiences severe disturbances, the rectifier needs to trip rapidly. This is associated with the rectifier real power decrease ramp-rate limit in normal operation, which is also typically set to a large value (corresponding to the green rising curve in Figure 13), allowing the load to be quickly transferred to the battery.

For rectifier reconnection, this process is effectively equivalent to reconnecting a load to the grid, and thus, the power ramp-up rate must be limited. This corresponds to the orange curve in Figure 13. The appropriate ramp rate depends on the rectifier trip duration, specifically, whether it is a fast reconnection following voltage recovery or a slower reconnection process, see Section 6.3.2.1 for more discussion.

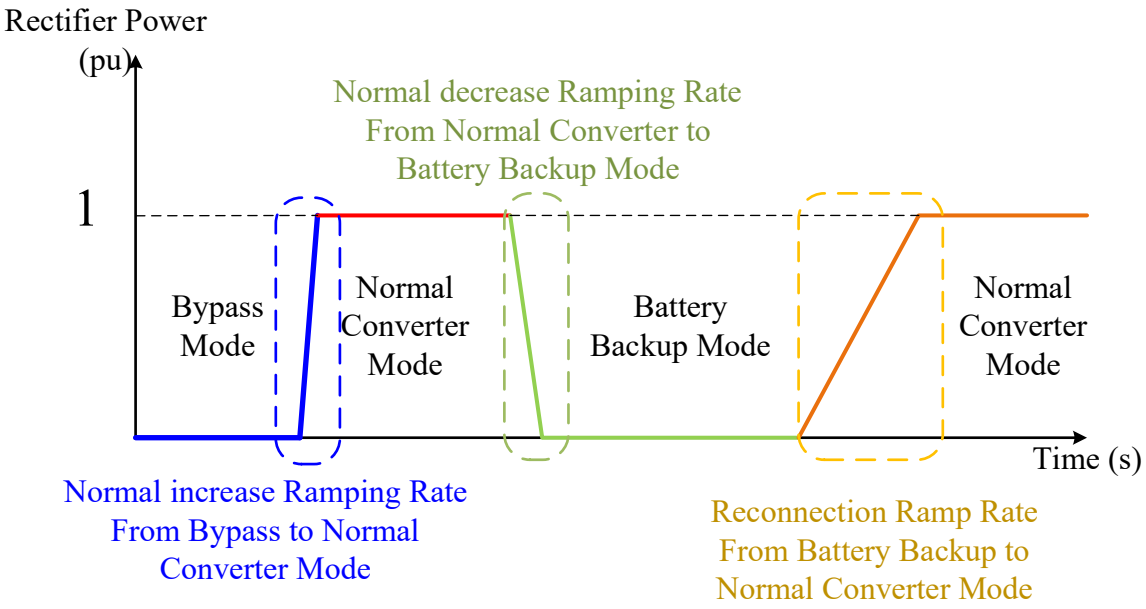


Figure 13: Definition of Rectifier ramping rate limitation.

For the q-axis current, a binary logic signal is also used to select the control mode, either reactive power (Q) control or AC voltage control. The corresponding reference value must be specified accordingly.

All PI controller parameters for both the outer power control loop and the inner current control loop are predefined within the model. However, users may modify these parameters if necessary.

3.4. Inverter

3.4.1. Main Circuit

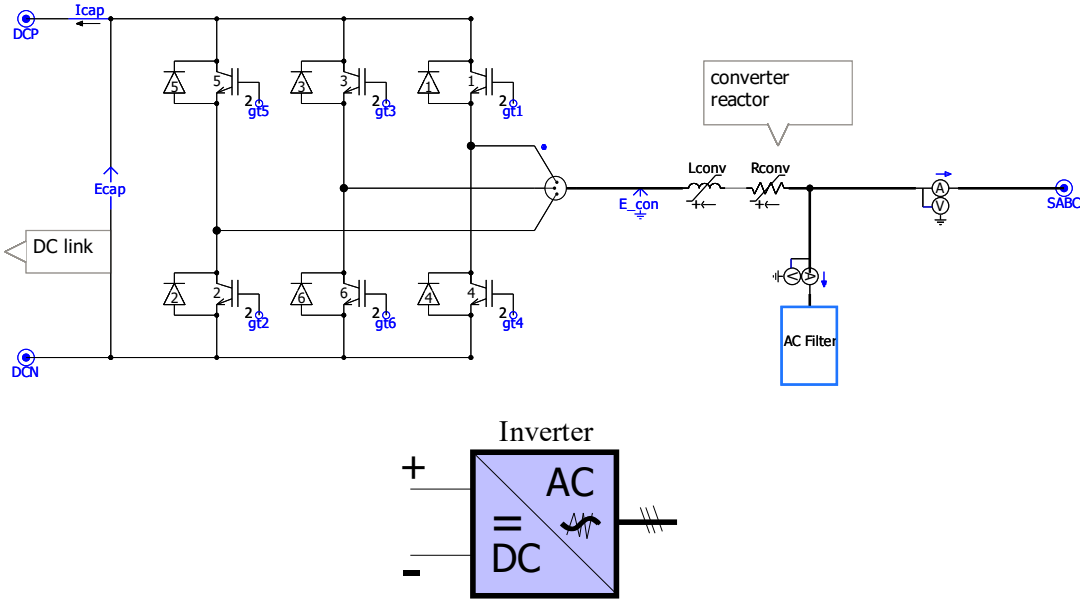


Figure 14: Main circuit and graphics of the inverter.

A three-phase, two-level voltage inverter in grid-forming (GFM) mode is used for the inverter to transfer the DC link voltage to AC voltage, which is usually 480V and 60Hz. Although the inverter output matches the utility grid in terms of nominal voltage and frequency, its power quality and reliability characteristics are inherently different. In particular, the inverter can maintain a stable voltage and frequency during grid disturbances or fault conditions, thereby enhancing system reliability. The main power circuit of the inverter is shown in Figure 14. The reference sine signal is generated based on the voltage from the proportional-integral (PI) controller and the reference frequency and then the sine wave is modulated to generate the PWM wave to control the Insulated-Gate Bipolar Transistor (IGBT) switching, a LC filter is used to filter out the high switching

frequency and then the AC voltage is connected to the single-phase power distribution units and PFC circuit in the server rack where the computing load is modelled as a constant power load.

3.4.2. LC Filter Parameters Calculation

The LC filter parameters are also calculated based on the rated capacity, voltage, and cutoff frequency. Refer to Section 3.3.2 for details.

3.4.3. Control Loop

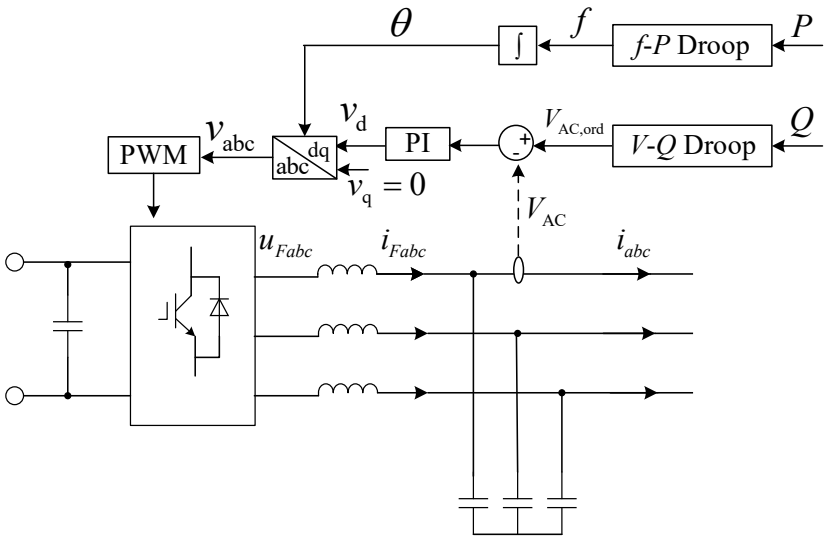


Figure 15: Inverter control diagram.

The inverter control architecture adopted in this work is illustrated in Figure 15, which is implemented in the dq-frame with the *P-f* and *Q-V* droop control.

3.4.3.1. Droop Control Loop

At the outer control layer, droop is employed to determine the inverter frequency f_{droop} and voltage magnitude $V_{\text{AC,droop}}$ based on the measured active, reactive power outputs and the DC link voltage, as shown in Figure 16.

$$f_{\text{droop}} = [1 + D_{\text{pf}}(P_{\text{set}} - P_{\text{GS,measure}})]f_{\text{ref}}, \tag{3.4}$$

$$V_{\text{AC,droop}} = [1 + D_{\text{qV}}(Q_{\text{set}} - Q_{\text{GS,measure}}) + D_{V_{\text{AC}}-V_{\text{DC}}}(V_{\text{DC,measure}} - V_{\text{DC,ord}})]V_{\text{AC,ord}}. \tag{3.5}$$

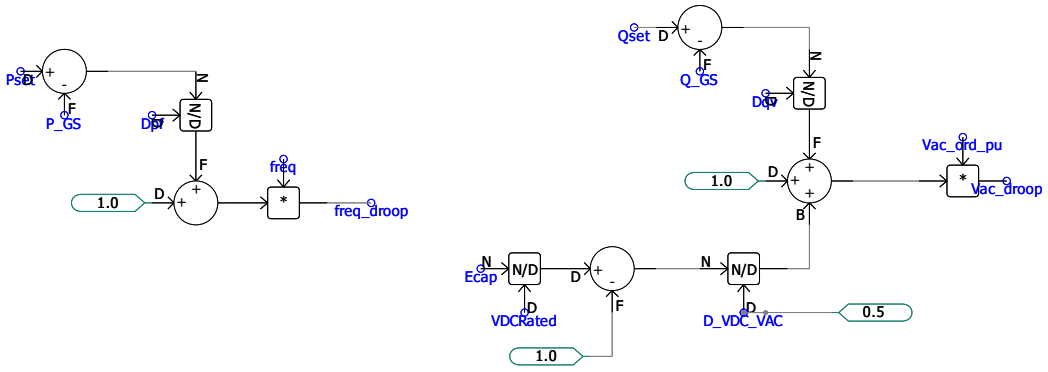


Figure 16: Inverter *P-f*, *Q-V,* and $V_{AC} - V_{DC}$ droop control.

1) *P-f* droop adjusts the output frequency according to the active power deviation.
2) *Q-V* droop regulates the voltage magnitude based on the reactive power deviation.

This droop control strategy enables the power synchronization of the inverter to the grid and achieves seamless transition from bypass mode to normal converter mode. It also allows decentralized power sharing among parallel UPS units without requiring communication.

Furthermore, considering the stability of the DC-link voltage and the dependence of the computing load behind the inverter on the AC voltage magnitude, a $V_{AC} - V_{DC}$ droop control is introduced. Specifically, when the DC-link voltage drops, the AC-side voltage supplied to the computing load is intentionally reduced, thereby decreasing the load demand and helping maintain DC-link voltage stability.

3.4.3.2. Voltage Control Loop

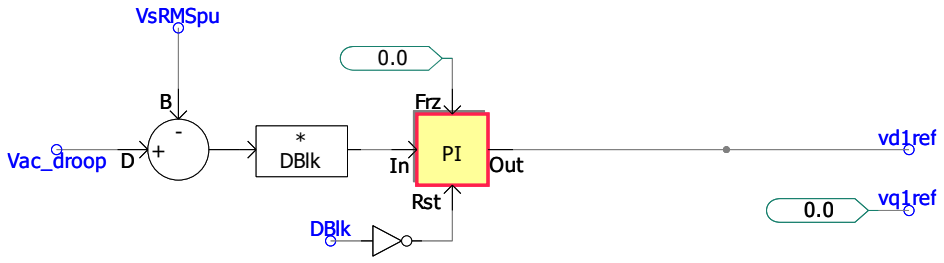


Figure 17: Single-loop voltage magnitude control in PSCAD.

The droop controls generate the reference frequency and voltage magnitude for the inverter. The reference frequency is integrated to obtain the phase angle used for the coordinate transformation between the abc-frame and dq-frame. The measured output voltages are transformed into a synchronous frame and compared with the reference values. The resulting voltage errors are processed by PI controllers to generate the voltage modulation commands in the dq-frame, as shown in Figure 17.

3.4.3.3. PWM-level Current Saturation Method

The current saturation is achieved in the PWM level based on the current clipping-based saturation [15] as shown in Figure 18. This control layer operates at the switching level and directly supervises the instantaneous phase currents of the inverter.

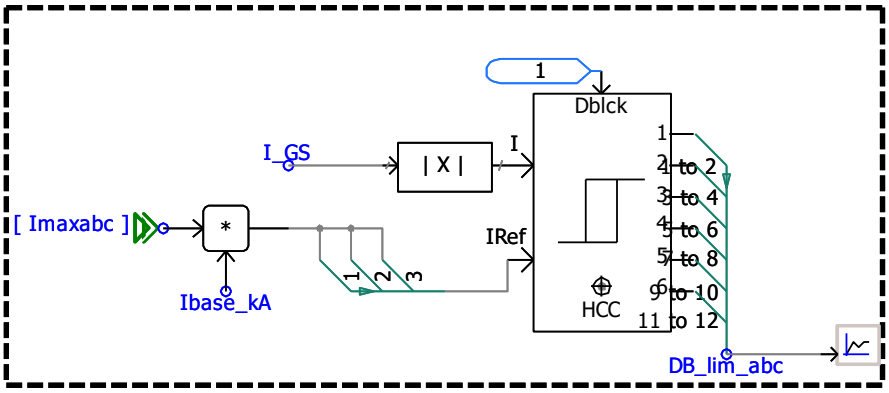


Figure 18: Current clipping-based saturation.

The three-phase inverter currents i_{abc} are continuously measured and compared with a predefined current limit I_{max}. The measured currents are normalized with respect to the base current I_{base} to obtain the per-unit current signal. If the magnitude of the inverter current exceeds the allowable limit, the protection logic activates a current blocking mechanism.

The current limiting logic generates a blocking signal “DB_lim_abc”, which is sent to the hysteresis-current control module of the PWM system. Once triggered, this signal temporarily blocks or modifies the PWM gating pulses of the inverter switches, preventing further increase of the inverter current. As a result, the inverter current is constrained

within a safe operating range, protecting the semiconductor devices (e.g., IGBTs/MOSFETs) and other power components.

The PWM-level current control operates independently of the outer voltage and power control loops and acts as a fast protection layer with a response time on the order of the switching period. This ensures that sudden disturbances such as load short circuits, transient faults, or large inrush currents do not cause excessive current stresses in the inverter.

3.4.4. Parameters

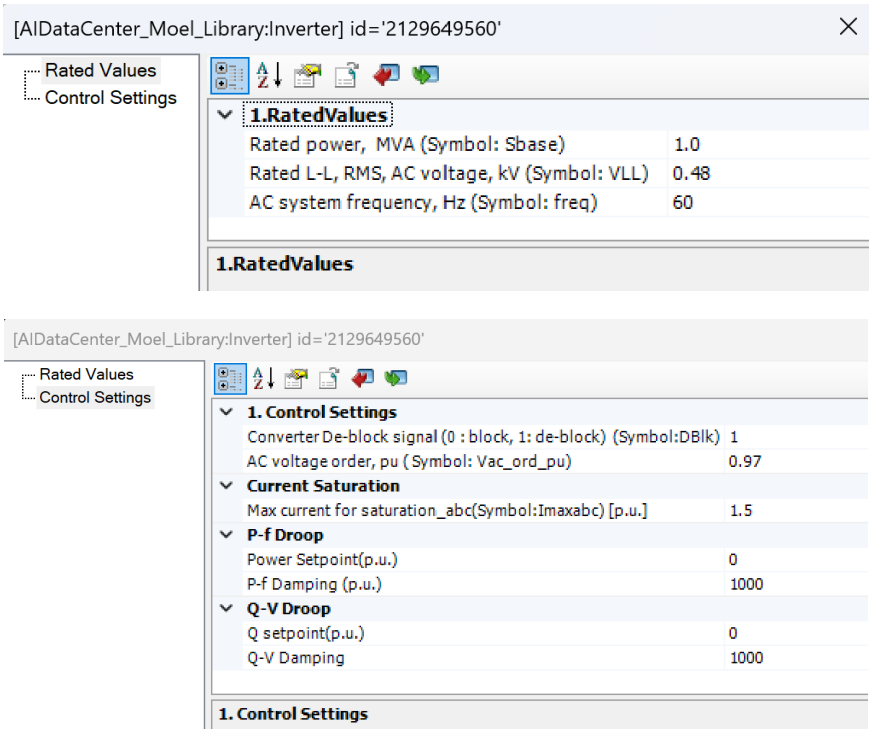


Figure 19: Control parameters of the inverter.

The parameters of the inverter are shown in Figure 19. The rated parameters are the same as the rectifier, which include the rated power, voltage, and frequency. The inverter control is configured through several key parameters that determine its operating condition and control behavior. The converter de-block signal determines whether the inverter is enabled or blocked. When the signal is set to 1, the inverter operates normally, while a value of 0 blocks the switching signals.

The AC voltage order specifies the reference value for the inverter output voltage. This value acts as the voltage setpoint for the inverter control and determines the target voltage magnitude at the output.

A PWM-level current saturation limit is implemented to protect the converter from excessive current. The maximum allowable phase current is defined by the current limit parameter. When the inverter current exceeds this limit, the controller activates current limiting to prevent damage to the power electronic devices.

The inverter also uses *P-f* droop and *Q-V* droop control to regulate active and reactive power. The *P-f* droop adjusts the inverter frequency based on active power changes, while the *Q-V* droop adjusts the voltage magnitude according to reactive power. The damping parameters (in per unit value) determine the sensitivity of frequency and voltage to power variations and influence the dynamic response of the inverter.

3.5. Bidirectional DC/DC

3.5.1. Main Circuit

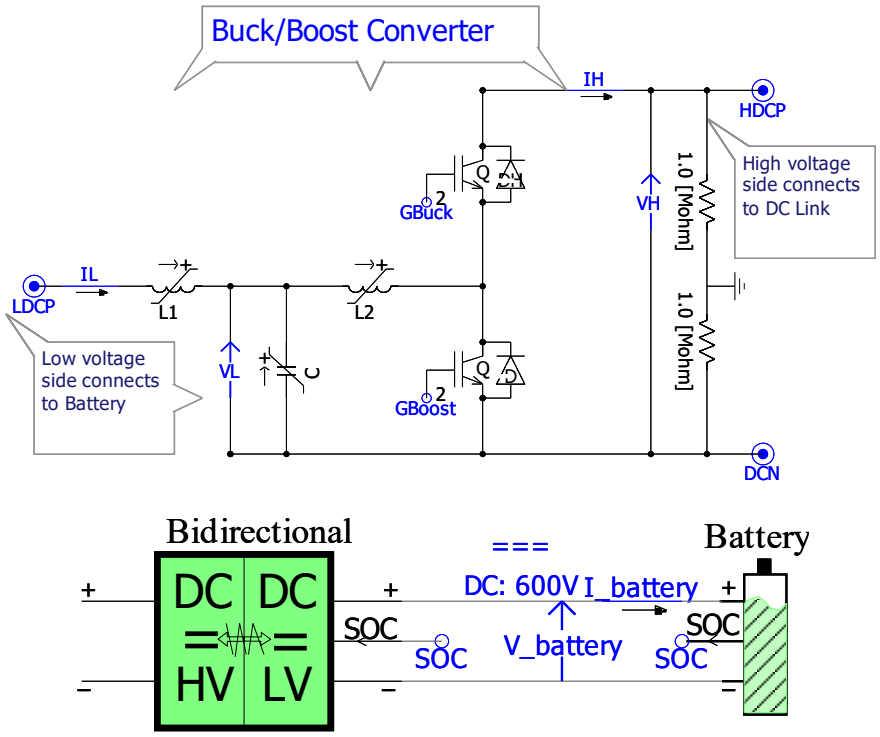


Figure 20: Main circuit of the buck/boost bidirectional DC/DC converter.

The main power circuit of the buck/boost bidirectional DC/DC converter is shown in Figure 20. It interfaces the battery with the DC link of the inverter. The low-voltage side of the converter is connected to the battery, while the high-voltage side is connected to the DC link supplying the inverter.

This converter enables bidirectional power flow depending on the UPS operating condition. During normal operation, when external power is available, it operates in the **buck mode** to charge the battery by stepping down the DC link voltage. During a grid outage, it switches to the **boost mode**, drawing energy from the battery and stepping up the battery voltage to maintain the required DC link voltage.

The converter consists of two controlled switches and an inductor to regulate power exchange between the battery and the DC link. By adjusting the switching signals, it

controls the battery charging and discharging currents while maintaining a stable DC link voltage.

Overall, the bidirectional DC/DC converter facilitates efficient energy exchange between the battery and the inverter DC link, enabling seamless transitions between charging and backup operation while ensuring reliable system performance.

3.5.2. Inductor and Capacitor Design

To decouple the battery from the converter's high-frequency switching dynamics, an LC filter comprising L1 and C is incorporated in conjunction with the main inductor L2 in the buck/boost circuit. The parameters of L1, L2, and C are automatically calculated based on the rated system values. The corresponding automatic calculation method implemented in PSCAD is illustrated in Figure 21.

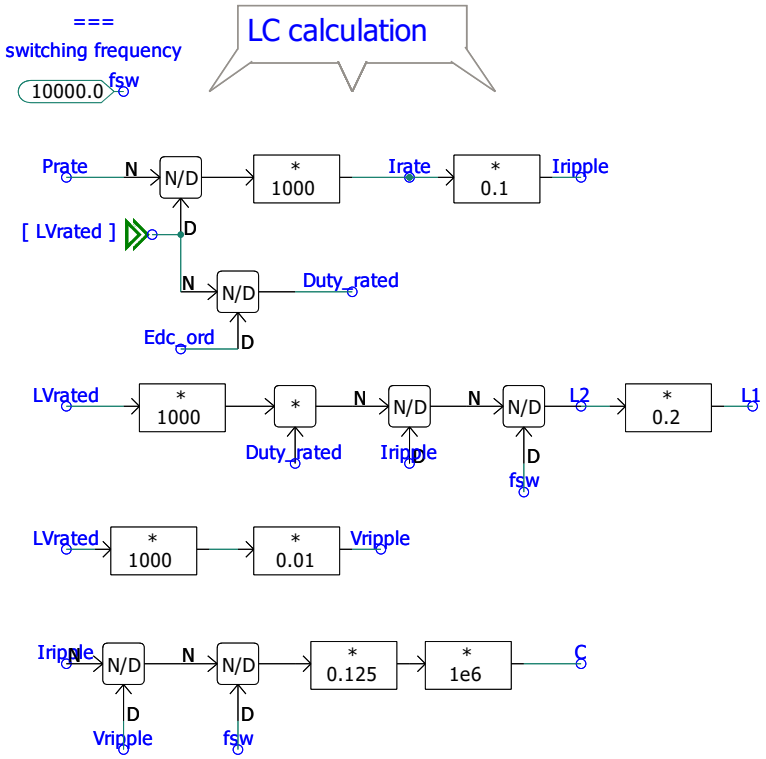


Figure 21: Inductor and capacitor automatic calculation in PSCAD.

Given the nominal voltages on the low- and high-voltage sides, denoted by V_{L}^{*} and V_{H}^{*}, and the rated power P_{rated}, the inductor current ripple is calculated according to (3.6).

$$I_{\text{ripple}} = 0.1 \times \frac{P_{\text{rated}}}{V_L^*}, \tag{3.6}$$

where the factor 0.1 corresponds to a preset current ripple of 10%.

The nominal duty ratio is determined based on the voltage ratio of the two sides:

$$D_{\text{average}} = \frac{V_{\text{L}}^*}{V_{\text{H}}^*}. \tag{3.7}$$

The main inductor L2 in the buck/boost circuit is then calculated as:

$$L_2 = \frac{V_{\text{L}}^* D_{\text{average}}}{f_{\text{sw}} I_{\text{ripple}}}, \tag{3.8}$$

where f_{sw} is the preset switching frequency.

The auxiliary inductor L1 is used to further reduce current ripple and is therefore selected as a fraction of L2, i.e. $L_1 = 0.2L_2$.

The capacitor value is determined based on a preset voltage ripple, chosen as 1% of the battery-side voltage, i.e., $V_{\text{ripple}} = 0.01V_{\text{L}}^*$. Accordingly, the capacitance is calculated as (3.9):

$$C = \frac{I_{\text{ripple}}}{8 f_{\text{sw}} V_{\text{ripple}}}. \tag{3.9}$$

3.5.3. Control Loop

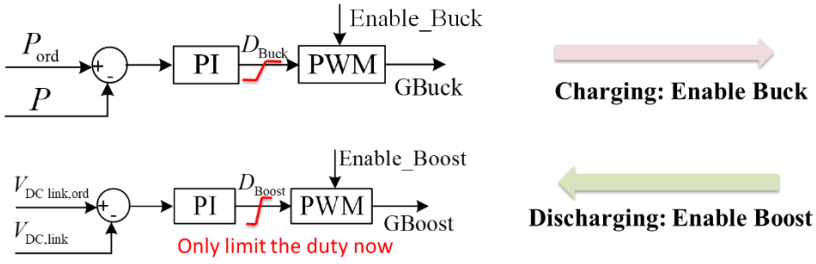


Figure 22: Control loop of the bidirectional DC/DC converter.

The bidirectional buck/boost converter is controlled using two independent current control loops to regulate the power flow between the battery and the DC link, as shown in Figure

22. Each direction of power transfer is governed by a dedicated PI controller, enabling seamless transition between charging and discharging modes.

3.5.3.1. Buck Mode for Battery Charging

In **charging operation (buck mode),** power flows from the DC link to the battery. The charging power is controlled through a PI controller, as illustrated in Figure 23. The reference charging current is compared with the measured inductor current, and the error is processed by a PI controller. The controller output is then modulated through a PWM module to generate the switching signals for the buck switch.

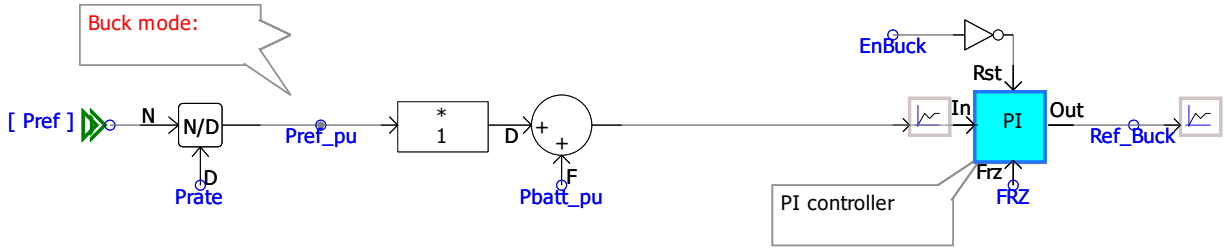


Figure 23: Buck mode and battery charging power control.

3.5.3.2. Boost Mode for Battery Discharging

In **discharging operation** (**boost mode)**, power flows from the battery to the DC link to support the inverter during grid outages. The DC link voltage is controlled in boost mode, as shown in Figure 24.

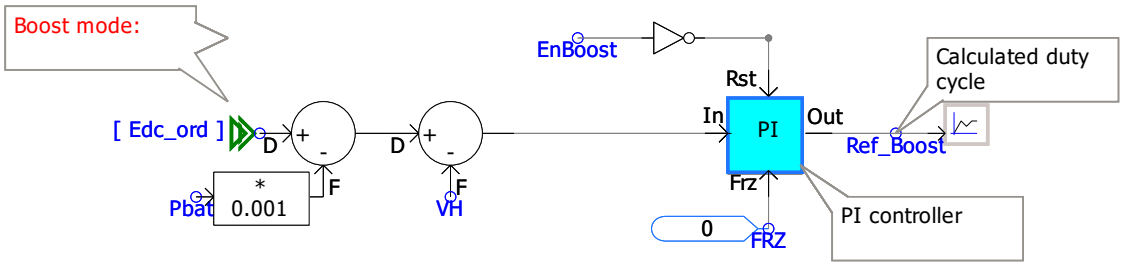


Figure 24: Boost mode and battery discharging control for DC link voltage.

3.5.4. Parameters

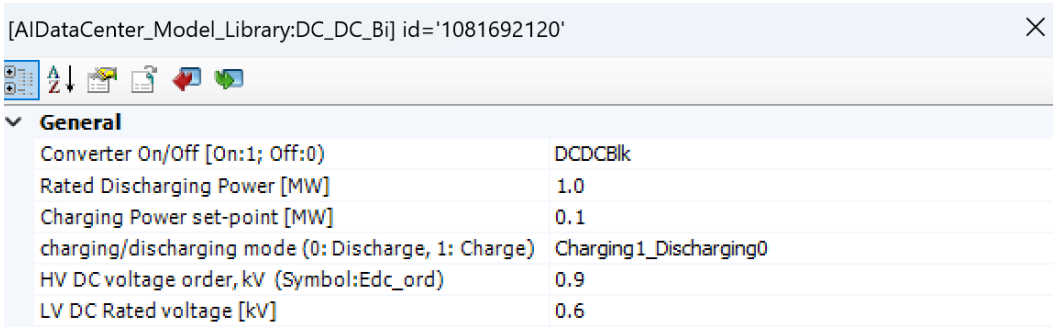


Figure 25: Parameter settings of DC/DC converter.

The parameters of the bidirectional DC/DC converter are shown in Figure 25.

The **converter on/off** setting determines whether the DC-DC converter is active. A value of 1 enables the converter, while a value of 0 disables its operation.

The **rated discharging power** specifies the maximum discharging power of the converter and should be set equal to or larger than the rated computing load.

The **charging power setpoint** defines the desired battery charging power. The converter regulates its operation to track this reference. The maximum allowable value should not exceed the difference between the rectifier rated power and the rated computing load.

The **charging/discharging mode** determines the direction of power flow. In charging mode (value = 1), power flows from the DC link to the battery. In discharging mode (value = 0), energy stored in the battery is delivered to the DC link to support the inverter.

The **HV DC voltage order** specifies the reference value of the DC link voltage during battery discharging (boost mode). When the battery supplies power to the system, the converter operates in boost mode to regulate the DC link voltage to this reference value.

The **LV DC rated voltage** should be set to the battery's nominal voltage.

3.6. Battery

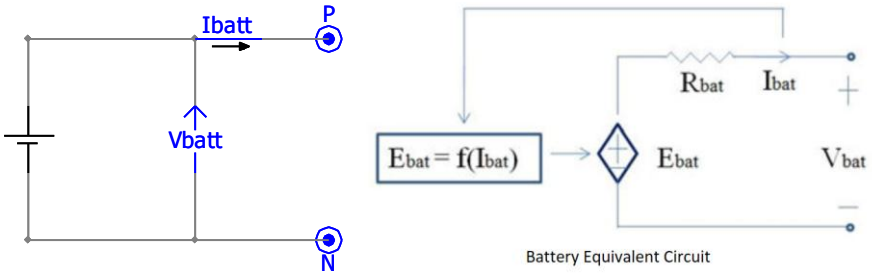


Figure 26: Equivalent circuit of the battery.

The battery circuit is shown in Figure 26. In this model, the battery is not represented as an ideal DC voltage source. Instead, the PSCAD library-based battery model is employed, which consists of an internal DC source and output resistance. The internal voltage varies as a function of the output current, capturing the non-ideal electrical behavior of the battery. In addition, the model provides a state-of-charge (SOC) signal to represent the battery energy level. The corresponding battery parameters are shown in Figure 27.

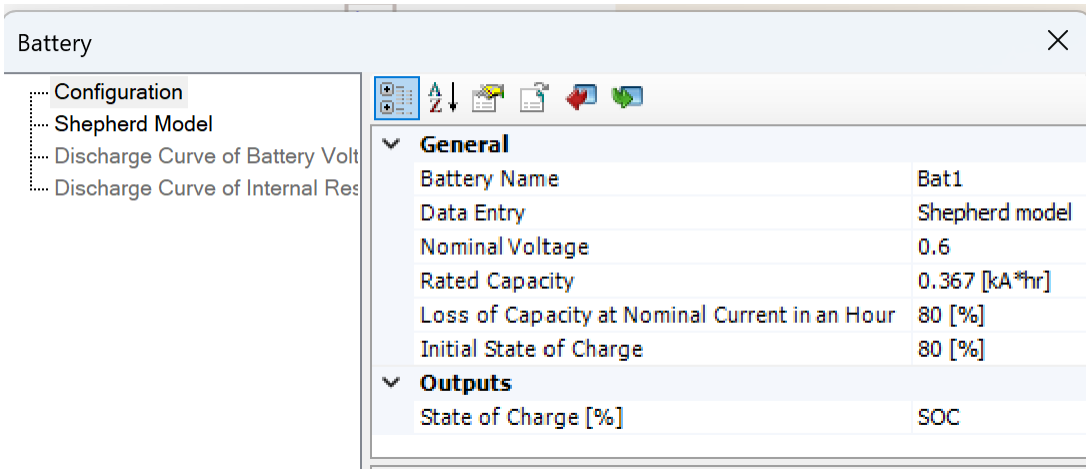


Figure 27: Parameters of the UPS battery.

3.7. VFD-Based Cooling Load

Data center cooling technologies can generally be categorized into air cooling, liquid cooling, and hybrid cooling [2]. The associated cooling loads are typically driven by electric motors powering fans and/or pumps. In modern data centers, these motors are usually not directly connected to the grid; instead, they are commonly supplied through VFD to enable efficient speed control and energy management.

A typical VFD consists of an AC/DC rectifier, a DC-link capacitor, and a DC/AC inverter. The rectifier converts the grid AC voltage into DC voltage and charges the DC-link capacitor, while the inverter regulates the motor voltage and frequency to control the motor speed and torque. The AC/DC rectifier can be implemented either as a diode-based rectifier or as a voltage-source-converter-based rectifier. Due to its simple control structure, lower cost, and lower losses, the diode-based rectifier is widely adopted in most VFDs for cooling applications.

On the inverter side, the motor is typically controlled using field-oriented control (FOC), which enables decoupled control of flux and torque, thereby allowing precise regulation of motor speed.

3.7.1. Main Circuit

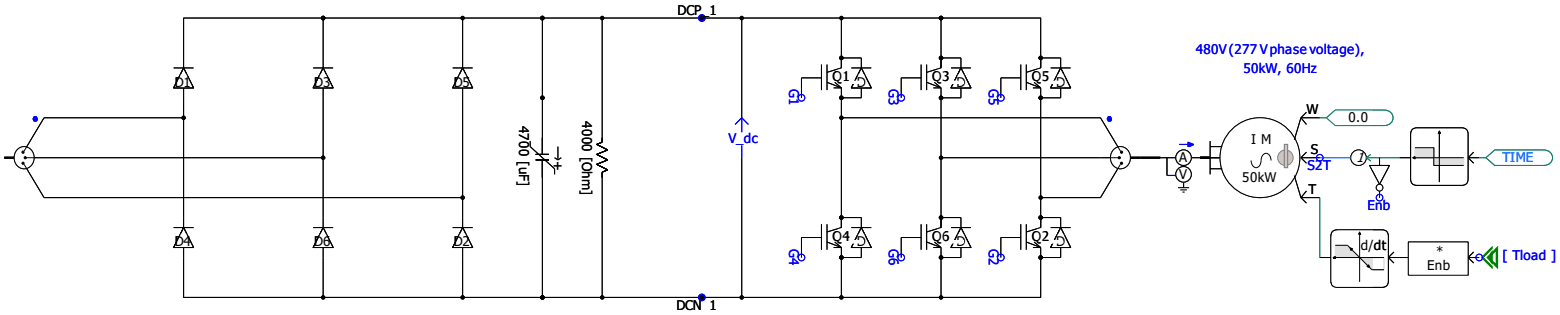


Figure 28: Main circuit of VFD-based cooling load.

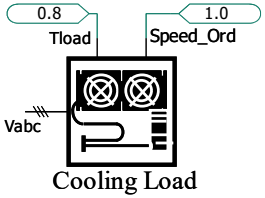


Figure 29: Graphic of the cooling load.

The variable frequency drive motor cooling load is illustrated in Figure 28, representing the electrically driven cooling system commonly used in modern AI data centers to dissipate the large amount of heat generated by high-power computing hardware. The corresponding PSCAD implementation is shown in Figure 29. The model takes the three-phase grid voltage as its electrical input, while the control input is the speed command of the cooling load. In addition, the real-time load torque applied to the motor must be specified. Users can define the functional relationship between motor speed and load torque to represent different cooling load characteristics.

In this configuration, the three-phase AC grid power is first processed by a power electronic drive consisting of a rectifier, a DC link, and an inverter. The rectifier converts the AC input to DC, while the DC link capacitor stabilizes the DC voltage. The inverter then generates a variable-frequency, variable-voltage three-phase output to drive an induction motor. By adjusting the inverter switching and output frequency, the motor speed can be continuously regulated.

The motor typically drives cooling equipment such as compressors, pumps, or large air-handling fans used in data center cooling systems. Since the motor speed can be modulated according to the cooling demand, VFD-based cooling loads offer high efficiency and flexible power consumption. However, they also behave as power-electronic loads, introducing fast dynamics and potential interactions with the power grid. This behavior is particularly important when analyzing the stability and load characteristics of AI data center power systems.

3.7.2. Control Loop

3.7.2.1. Motor Speed Control

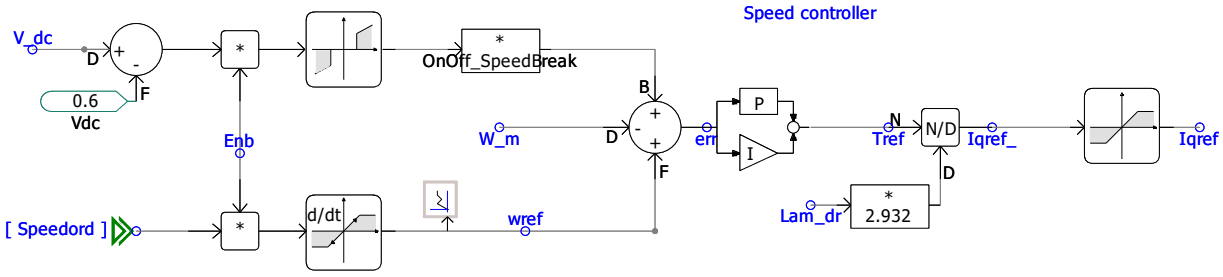


Figure 30: Speed control loop of VFD motor-based cooling load.

A three-phase inverter is used to drive the VFD induction motor. The control strategy is based on FOC, in which the q-axis current regulates the motor torque and, consequently, the rotor speed. The speed control loop associated with q-axis is illustrated in Figure 30. The control structure is composed of several functional blocks that generate the inverter switching signals based on the measured motor variables. Specifically, the speed controller compares the reference speed with the measured rotor speed, and the resulting speed error is processed by a PI controller to produce the torque-producing current

reference. This reference determines the electromagnetic torque required for the motor to track the desired speed.

3.7.2.2. Stator Flux Angle Calculation

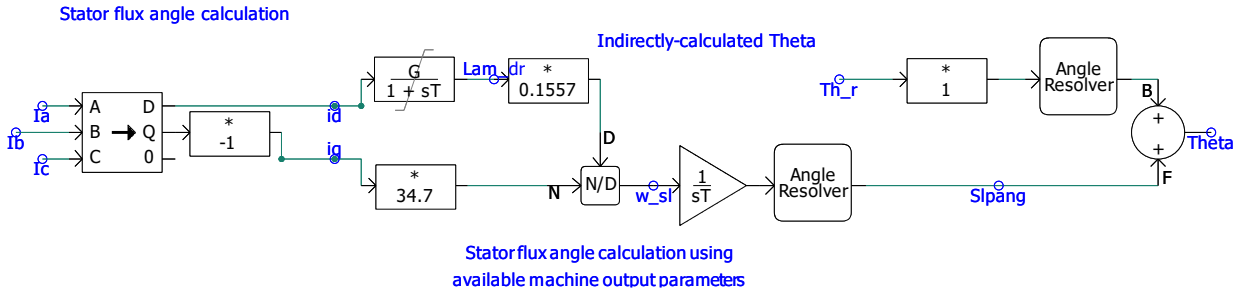


Figure 31: Stator flux angle calculation in PSCAD.

The stator flux angle calculation block estimates the stator flux vector and its angular position, as shown in Figure 31. Using the measured stator currents and motor parameters, the stator flux is obtained through a dynamic model of the machine. The flux angle is then computed and used to align the rotating reference frame. This step is essential for field-oriented control as it enables the stator currents to be decomposed into flux-producing and torque-producing components, thereby achieving decoupled control of flux and torque.

The synchronous electrical angular speed is

$$\omega_e = \omega_r + \omega_{sl}, \tag{3.10}$$

where ω_e is synchronous electrical angular speed; ω_r is rotor electrical speed; ω_{sl} is the slip angular speed.

The flux angle is obtained by integrating the electrical speed:

$$\theta = \int \omega_e dt$$
$$\text{i.e., } \theta = \int \omega_r + \omega_{sl} dt \tag{3.11}$$

For a squirrel-cage induction motor, the slip frequency used in FOC is:

$$\omega_{sl} = \frac{R_r}{L_r}\frac{i_q}{i_d}, \tag{3.12}$$

where R_r is rotor resistance; L_r rotor inductance; i_d is d-axis current (flux producing); i_q is q-axis current (torque producing).

The **indirect flux angle** used for the dq-transformation is:

$$\theta = \int (\omega_r + \frac{R_r}{L_r}\frac{i_q}{i_d})dt\,. \tag{3.13}$$

Based on the torque command from the speed controller and the desired flux level, the d-axis and q-axis current references are generated.

3.7.2.3. Hysteresis Current Control

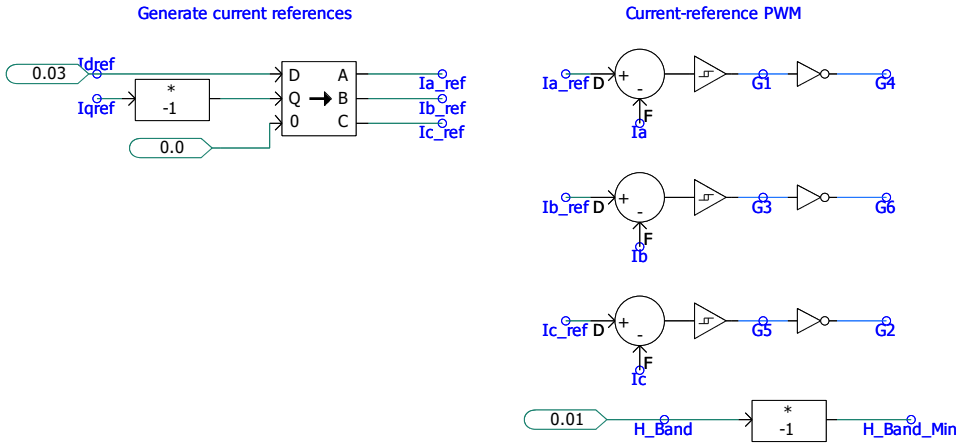


Figure 32: Current-controlled PWM (hysteresis current control).

The hysteresis current control shown in Figure 32 is employed for the motor current regulation, which differs from the conventional SPWM used in voltage-source inverter control. In this approach, a current-reference PWM or hysteresis current control scheme is adopted, where the difference between the reference current and measured current is processed to directly generate the switching signals for each inverter leg.

3.7.3. Parameters

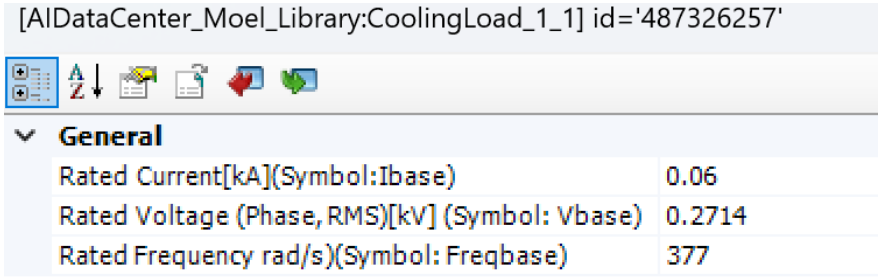


Figure 33: Parameters of VFD cooling load.

Figure 33 shows the base values used for the per-unit system in the induction motor model of the cooling load. These parameters define the normalization references for electrical quantities in the simulation.

3.8. Computing Load/IT load

Computing loads or IT loads are typically modeled as constant-power loads, with power profiles determined by the computing demand and the specific algorithms being executed. In AI data center modeling, two types of constant-power load models are provided, depending on whether the terminal interface is AC-connected or DC-connected, as shown in Figure 34.

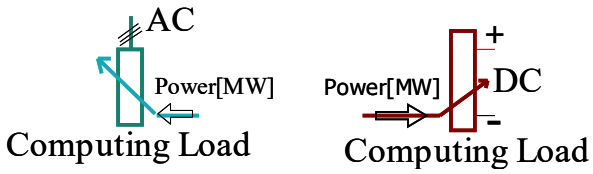


Figure 34: Computing load model in PSCAD.

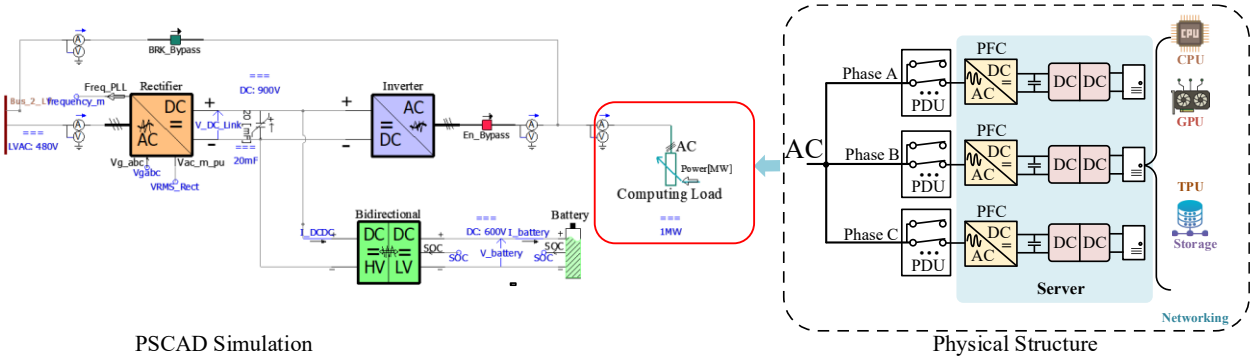


Figure 35: Schematic diagram of the aggregated three-phase AC-interface computing load.

The AC-interface computing load corresponds to the case where aggregation is performed at the three-phase AC terminals immediately after the inverter, as illustrated in Figure 35. In this configuration, each phase, including the PDU, PFC circuits, DC/DC converters, and GPU loads, is lumped into an equivalent three-phase constant AC load.

The implementation of the AC-connected load is illustrated in Figure 36. It is realized by dynamically adjusting the equivalent load resistance. Specifically, the resistance RLoad is controlled based on the real-time computing load profile PLoad and the measured RMS voltage Vm. In this method, during transients, the load still behaves as a constant impedance. A closed-loop control is then employed to regulate the power toward a constant value in real time, with the control bandwidth determined by the RMS voltage

filter. This approach effectively emulates the dynamic behavior of the PFC stage in regulating the DC-link voltage.

$$R_{\text{Load}} = \frac{V_{\text{RMS}}^{\ 2}}{P_{\text{Load}}}. \tag{3.14}$$

It is important to note that the AC-connected load represents the aggregation of all PFC units downstream of the inverter. Due to the presence of a large DC-link capacitor following each PFC stage, the AC-connected load does not behave as a perfect constant power load during transients, but instead exhibits a control delay. This effect can be emulated by introducing a filter on the measured AC RMS voltage, where the filter time constant corresponds to the bandwidth of the PFC voltage control loop after the inverter, typically in the range of 10–30 Hz.

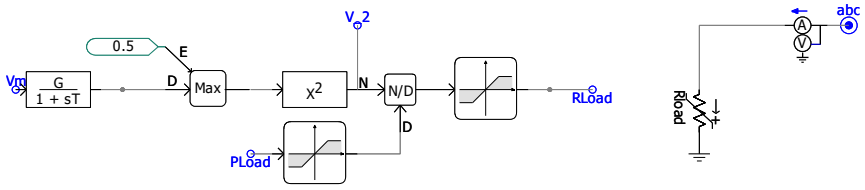


Figure 36: AC-connected computing load.

For the AC-connected computing load, the corresponding parameters include the rated AC voltage and frequency. The active can be controlled through a time-varying input signal “Power[MW]”, as shown in Figure 34, allowing load profiles to be directly specified to capture dynamic load fluctuations.

A more accurate way to model the computing load is to represent the DC load downstream of the PFC output capacitor as a constant power load. In this configuration, the inverter output is connected to a transformer, with each phase feeding a single-phase PFC unit. The DC computing load is then connected at the output of the PFC stage. If single-phase PFC circuits are present on each phase after the inverter or the utility grid, and the aggregation is performed downstream of the PFC stage, the load should instead be modeled as a constant power load using the DC-interface computing load, as shown in Figure 37.

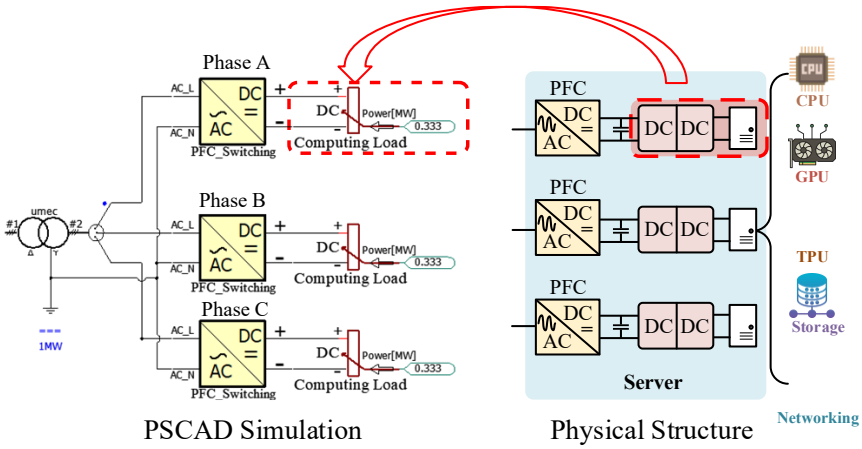


Figure 37: Schematic diagram of the aggregated DC-interface computing load after single-phase PFC.

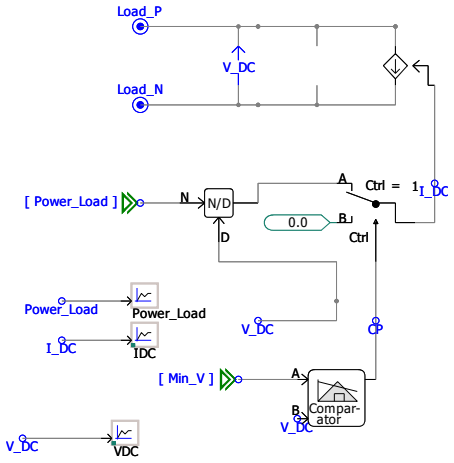


Figure 38: DC-connected constant power load.

The DC-connected constant power load is modeled as shown in Figure 38, using a controlled current source to represent an ideal constant DC load. Specifically, the current is computed as:

$$i = \frac{P_{\text{Load}}}{V_{\text{DC}}}. \tag{3.15}$$

For the DC-connected constant-power load, a control signal is used to define the dynamic load behavior. Specifically, the load profile can be represented as a time-varying signal and applied to the “Power[MW]” signal input port, enabling flexible modeling of time-dependent power demand.

In a double-conversion UPS architecture, the voltage downstream of the inverter depends on the operating mode. In bypass mode, it is determined by the grid voltage, whereas in normal converter mode and battery backup mode, it is regulated by the inverter output voltage. Once small disturbances occur in the grid voltage, the inverter rapidly takes over the load. Therefore, the AC voltage downstream of the inverter and upstream of the PDU can be considered nearly constant. As a result, in a double-conversion UPS-based AI data center, the downstream loads of the inverter can be aggregated as a constant power load, i.e., represented using a three-phase AC-interfaced computing load.

4. Average Models of Power Converters

Since most grid studies focus on low-frequency system-level stability rather than high-frequency switching behavior, which is related to device-level design, average models are developed for all power converters. This section presents the implementation of these average models for power converters, including the rectifier, inverter, bidirectional DC/DC converter, and VFD. Furthermore, a comparison between the average and switching models is provided in terms of dynamic performance and simulation efficiency.

4.1. Average Models of Rectifier and Inverter

The rectifier and inverter both employ three-phase, two-level PWM voltage-source converters, and their average-value modeling approaches are identical; therefore, they are introduced together in this section.

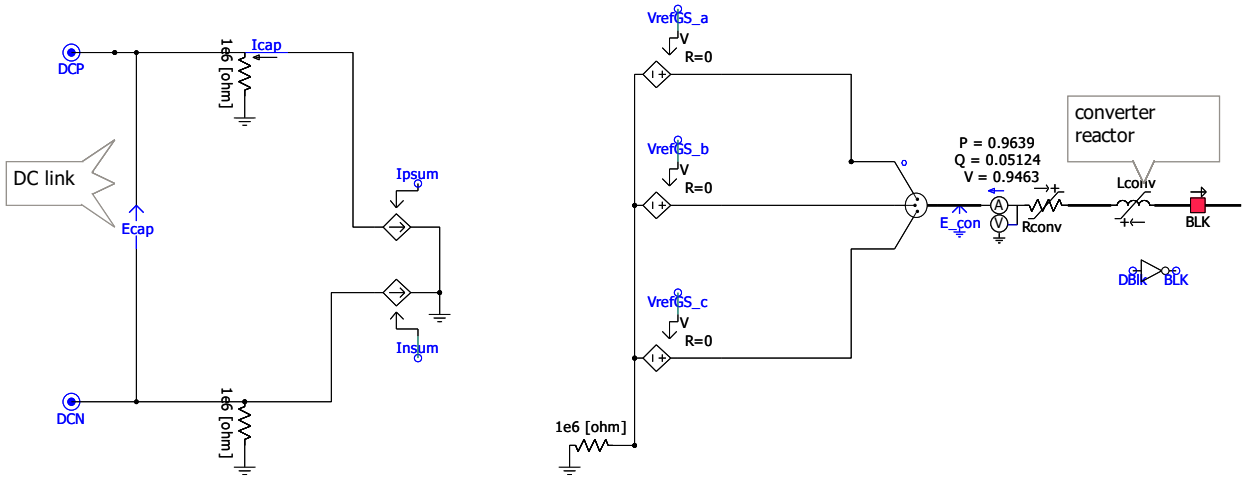


Figure 39: Average model of the rectifier and inverter.

On the AC side, the sinusoidal voltage reference generated by the PI control loop is directly applied to a controlled voltage source to produce the AC output voltage. To transfer power to the DC side, the measured three-phase instantaneous currents on the AC side are used to compute the corresponding DC-side current. The overall average-value modeling approach for both the rectifier and inverter is illustrated in Figure 39. This approach eliminates explicit high-frequency switching while preserving the fundamental-

frequency power interaction between the AC system and the DC link, thereby significantly improving simulation efficiency for large-scale system studies.

In the average-value converter model, the DC-side current is determined based on the instantaneous power balance between the AC and DC sides. Specifically, the instantaneous AC power is calculated from the three-phase voltages and currents as:

$$p_{\mathrm{AC}} = v_{\mathrm{a}} i_{\mathrm{a}} + v_{\mathrm{b}} i_{\mathrm{b}} + v_{\mathrm{c}} i_{\mathrm{c}} . \tag{4.1}$$

Assuming an ideal converter without switching losses, the instantaneous AC power equals the DC power:

$$p_{\mathrm{AC}} = p_{\mathrm{DC}} = V_{\mathrm{DC}} I_{\mathrm{DC}} . \tag{4.2}$$

Therefore, the DC current injected into the DC link can be expressed as:

$$I_{\mathrm{DC}} = \frac{v_{\mathrm{a}} i_{\mathrm{a}} + v_{\mathrm{b}} i_{\mathrm{b}} + v_{\mathrm{c}} i_{\mathrm{c}}}{V_{\mathrm{DC}}} = 0.5 m_{\mathrm{abc}} \cdot i_{\mathrm{abc}} , \tag{4.3}$$

where m_{abc} are the three-phase modulation signals.

The modulation signals are converted into two complementary switching functions: $\frac{1+m_{\mathrm{abc}}}{2}$ and $\frac{1-m_{\mathrm{abc}}}{2}$, which represent the average connection ratios of each phase leg to the positive and negative DC rails, respectively. Based on these switching functions, the three-phase AC currents are distributed to the positive and negative DC-side currents, denoted by I_{p} and I_{n}.

Specifically, the following relationships hold:

$$I_{\mathrm{p}} = \frac{1+m_{\mathrm{abc}}}{2} i_{\mathrm{abc}}, I_{\mathrm{n}} = \frac{1-m_{\mathrm{abc}}}{2} i_{\mathrm{abc}} , \tag{4.4}$$

$$I_{\mathrm{p}} + I_{\mathrm{n}} = i_{\mathrm{a}} + i_{\mathrm{b}} + i_{\mathrm{c}} = 0 , \tag{4.5}$$

$$I_{\mathrm{DC}} = \frac{I_{\mathrm{p}} - I_{\mathrm{n}}}{2} . \tag{4.6}$$

Therefore, the DC-side current feedback is obtained from the average contribution of each phase current to the two DC rails, as illustrated in Figure 40.

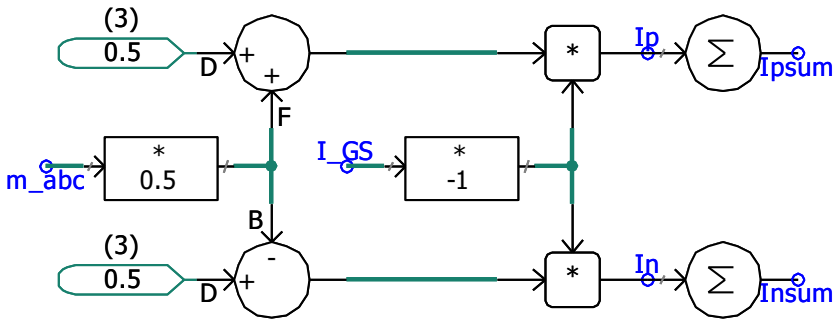


Figure 40: AC-DC current feedback method of the average model of the rectifier and inverter.

4.2. Average Model of Bidirectional DC/DC Converter

Figure 41 illustrates the average-value model of a bidirectional buck/boost DC/DC converter used to interface the battery with the DC link. The low-voltage side is connected to the battery, while the high-voltage side is connected to the DC-link bus of the UPS system.

To avoid simulating high-frequency switching dynamics, an average-value modeling approach is adopted. In this approach, the switching devices are replaced by controlled sources governed by duty ratios, which represent the averaged behavior of the converter over a switching period.

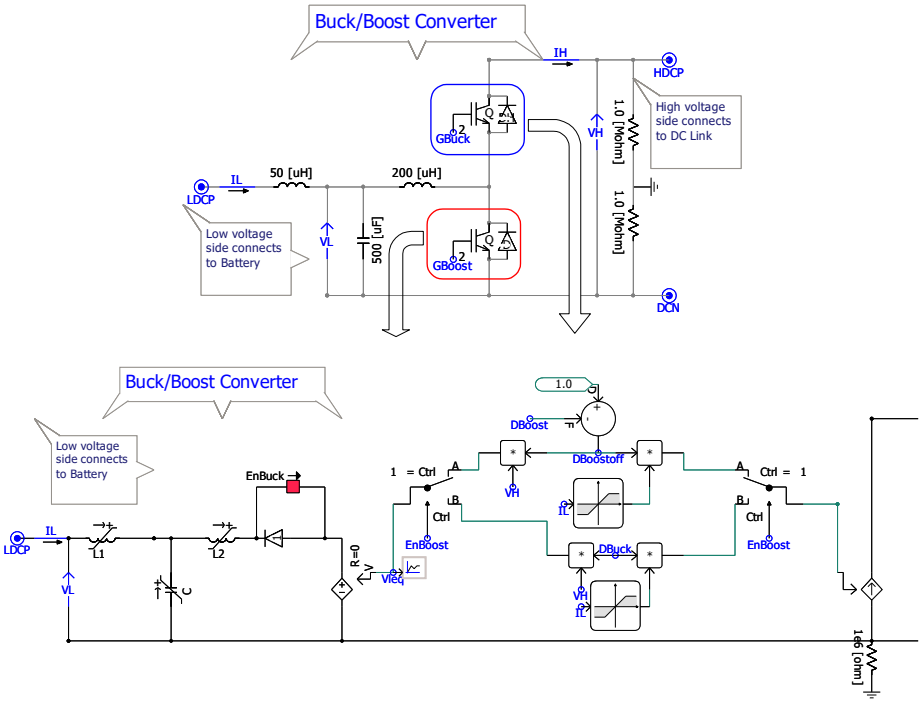


Figure 41: Average model of the bidirectional buck/boost converter.

The converter operates in two modes:

1) **Buck mode (charging mode)**: Power flows from the DC link to the battery. In this mode, the converter steps down the DC-link voltage and regulates the battery charging current. The charging power is controlled by adjusting the duty ratio D_{buck} in buck operation, which determines the low-voltage-side output voltage.

In buck mode, the low-voltage-side voltage is given by:

$$V_{\mathrm{L}} = D_{\mathrm{buck}} V_{\mathrm{H}} . \tag{4.7}$$

Accordingly, a controllable voltage source is used to impose V_{L} based on (4.7). The corresponding low-voltage-side current I_{L} is then reflected to the high-voltage side through a controllable current source, given by:

$$I_{\mathrm{H}} = D_{\mathrm{buck}} I_{\mathrm{L}} . \tag{4.8}$$

2) **Boost mode (discharging mode):** Power flows from the battery to the DC link. In this mode, the converter boosts the battery voltage to maintain the DC-link voltage during disturbances or when the rectifier power is unavailable.

The controllable voltage source on the high-voltage side is defined as:

$$V_{\mathrm{L}} = (1 - D_{\mathrm{Boost}}) V_{\mathrm{H}} , \tag{4.9}$$

and the corresponding current relationship is:

$$I_{\mathrm{H}} = (1 - D_{\mathrm{Boost}}) I_{\mathrm{L}} . \tag{4.10}$$

In the average model, additional constraints are imposed on the high-voltage-side current I_{H} and low-voltage-side current I_{L}, to ensure physically consistent power flow.

In buck mode, power flows from the high-voltage side to the low-voltage side; consequently, both I_{H} and I_{L} are negative. In boost mode, power flows from the low-voltage side to the high-voltage side, and I_{H} becomes positive. Hence, an upper bound and a lower bound limiter are added to I_{H} separately. To enforce these conditions, upper and lower bound limiters are applied to the current variables. In addition, a diode is included on the low-voltage side to ensure unidirectional conduction consistent with buck-mode operation.

4.3. Average Model of VFD

The average model of the VFD is shown in Figure 42. In this model, the three-phase, two-level full bridge is replaced by a controllable voltage source, and the measured AC-side currents are fed back to the DC side.

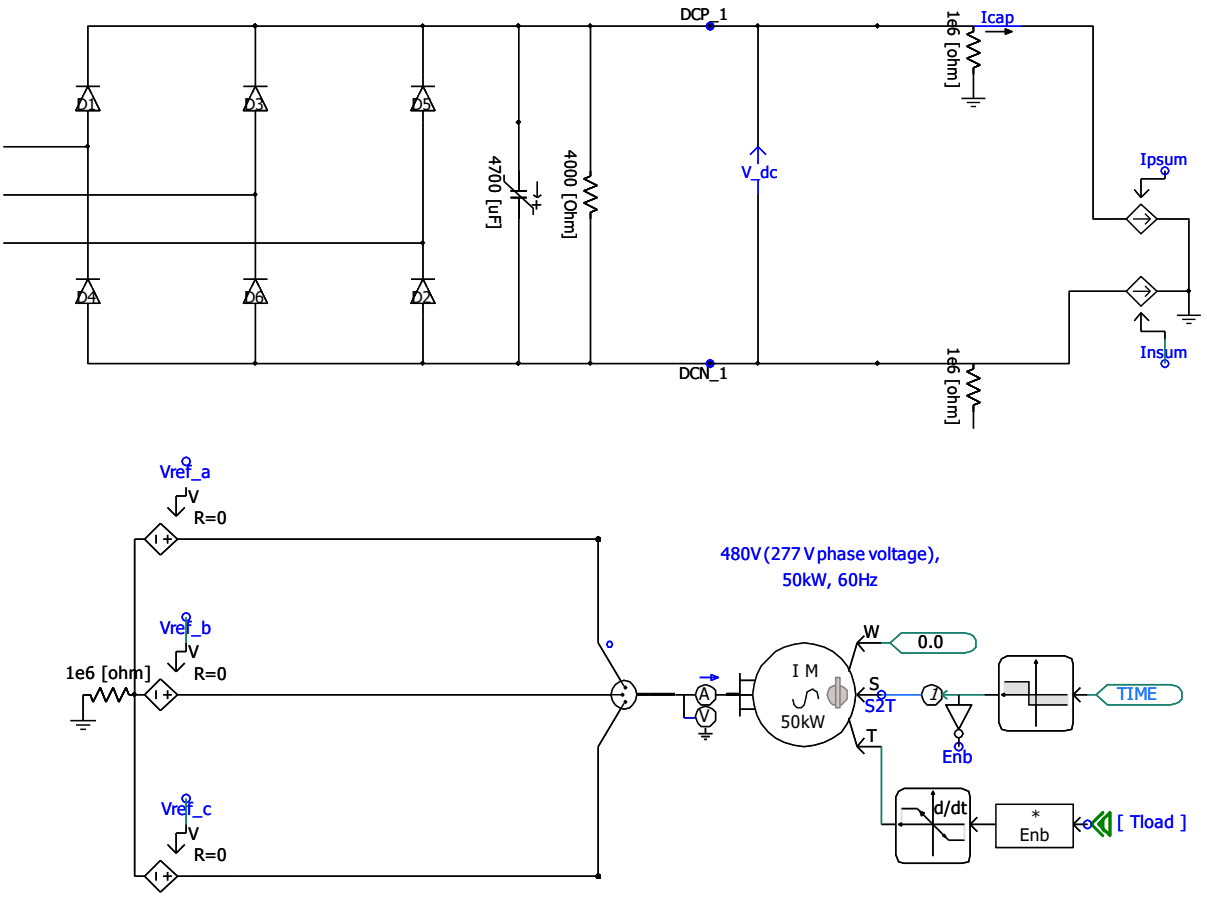


Figure 42: Average Model of VFD-Motor-based Cooling Load.

Since hysteresis current control does not operate at a fixed switching frequency, averaging over a switching period is not directly applicable. Therefore, the hysteresis current comparison block is retained in the average-value model, and the resulting switching signals (0 or 1) are used to determine the output voltage of the three-phase controllable voltage source. The AC voltage generation method is illustrated in Figure 43.

The reference currents i_a^{ref}, i_b^{ref}, and i_c^{ref} are compared with the measured phase currents i_a, i_b, i_c. The resulting current errors are processed by hysteresis comparators with a predefined hysteresis band. Based on the comparison results, binary switching signals are generated for each inverter leg (G1–G6 $\in \{0,1\}$), which determine the switching states of the upper and lower devices in the three-phase bridge. These switching states are then mapped to phase switching functions S_a, S_b and S_c, each taking values of -1 or +1. Finally, the phase voltages are obtained as:

$$v_{abc} = \frac{V_{DC}}{2} S_{abc}, \tag{4.11}$$

which serves as the outputs of the controllable voltage source.

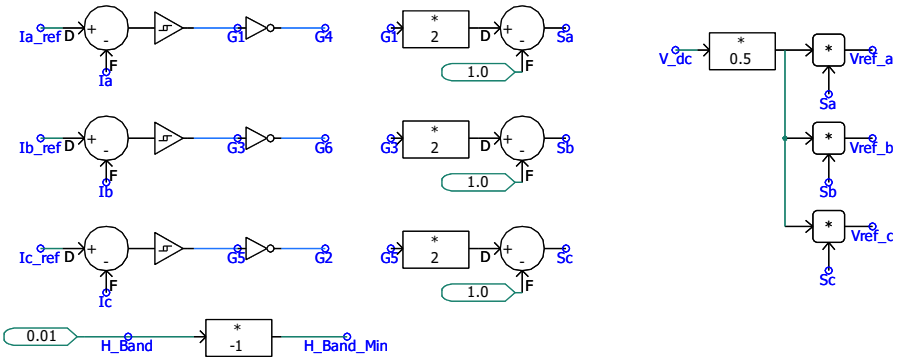


Figure 43: Average AC voltage generation of hysteresis current control.

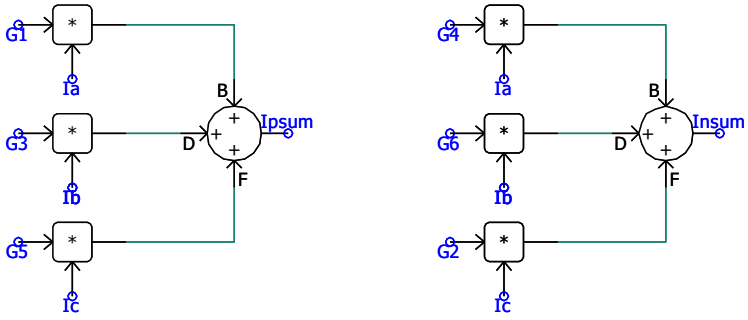


Figure 44: AC-DC current feedback method in the average model.

Figure 44 illustrates the calculation of the DC-side currents based on the switching states and the AC-side phase currents. The switching signals G1-G6 represent the on/off states of the upper and lower switches of the three-phase converter. These switching signals are multiplied by the corresponding phase currents and then summed up to obtain the DC-side current contribution.

Specifically, the current contributions from the upper switches (G1,G3,G5) are summed to obtain the positive DC current I_{p}, while the contributions from the lower switches (G4,G6,G2) are summed to obtain the negative DC current I_{n}.

$$\begin{aligned} I_{\mathrm{p}} &= G_1 i_{\mathrm{a}} + G_3 i_{\mathrm{b}} + G_5 i_{\mathrm{c}} \\ I_{\mathrm{n}} &= G_4 i_{\mathrm{a}} + G_6 i_{\mathrm{b}} + G_2 i_{\mathrm{c}} \\ G_k &\in \{0,1\}, k = 1,2...6 \end{aligned} \tag{4.12}$$

This formulation ensures power consistency between the AC and DC sides in the average-value converter model.

Finally, it is noted that, in this average model, only the switching dynamics of the IGBTs are removed. The high-frequency binary switching signals are retained to control the reference voltages of the controllable voltage sources.

4.4. Comparison Between Average and Switching Models

4.4.1. Dynamic Performance Comparison

Figure 45 and Figure 46 present a comparison between the switching model and the average model of the UPS under voltage disturbances. The results indicate that the two models exhibit nearly identical low-frequency dynamic responses.

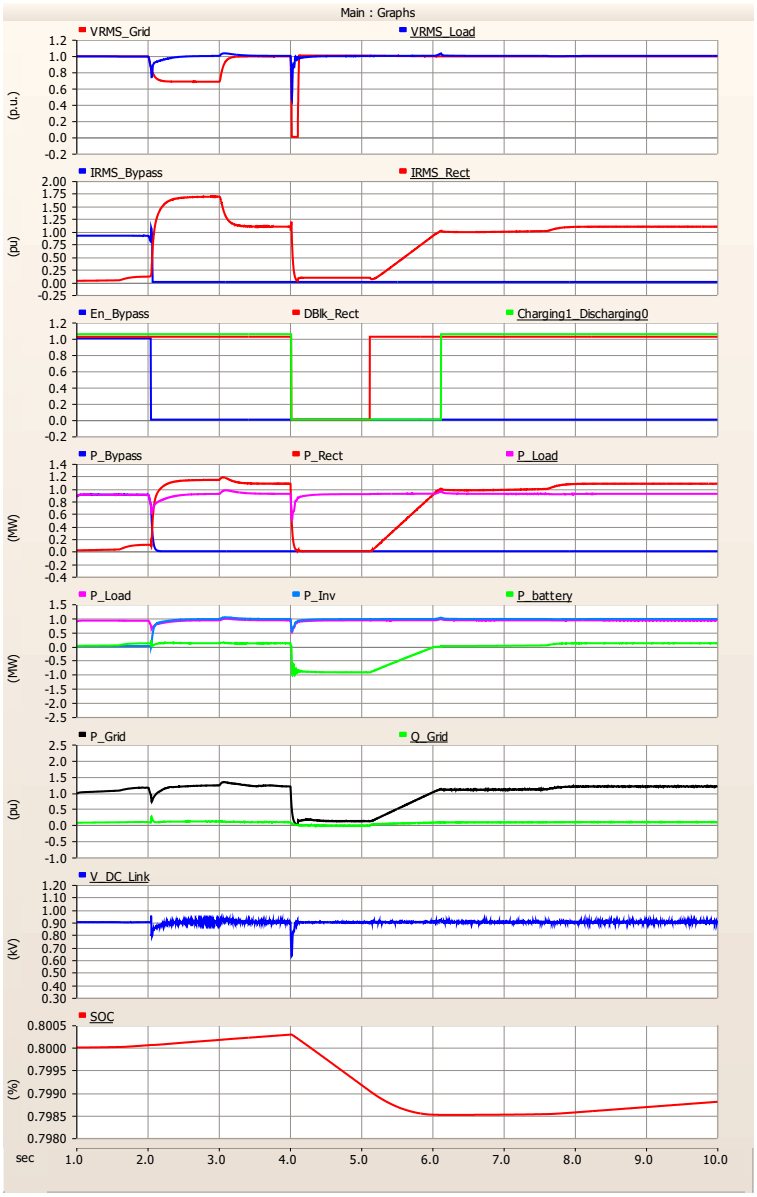


Figure 45: Dynamic results of UPS switching model under disturbance (simulation time step: 1us and switching frequency: 10kHz).

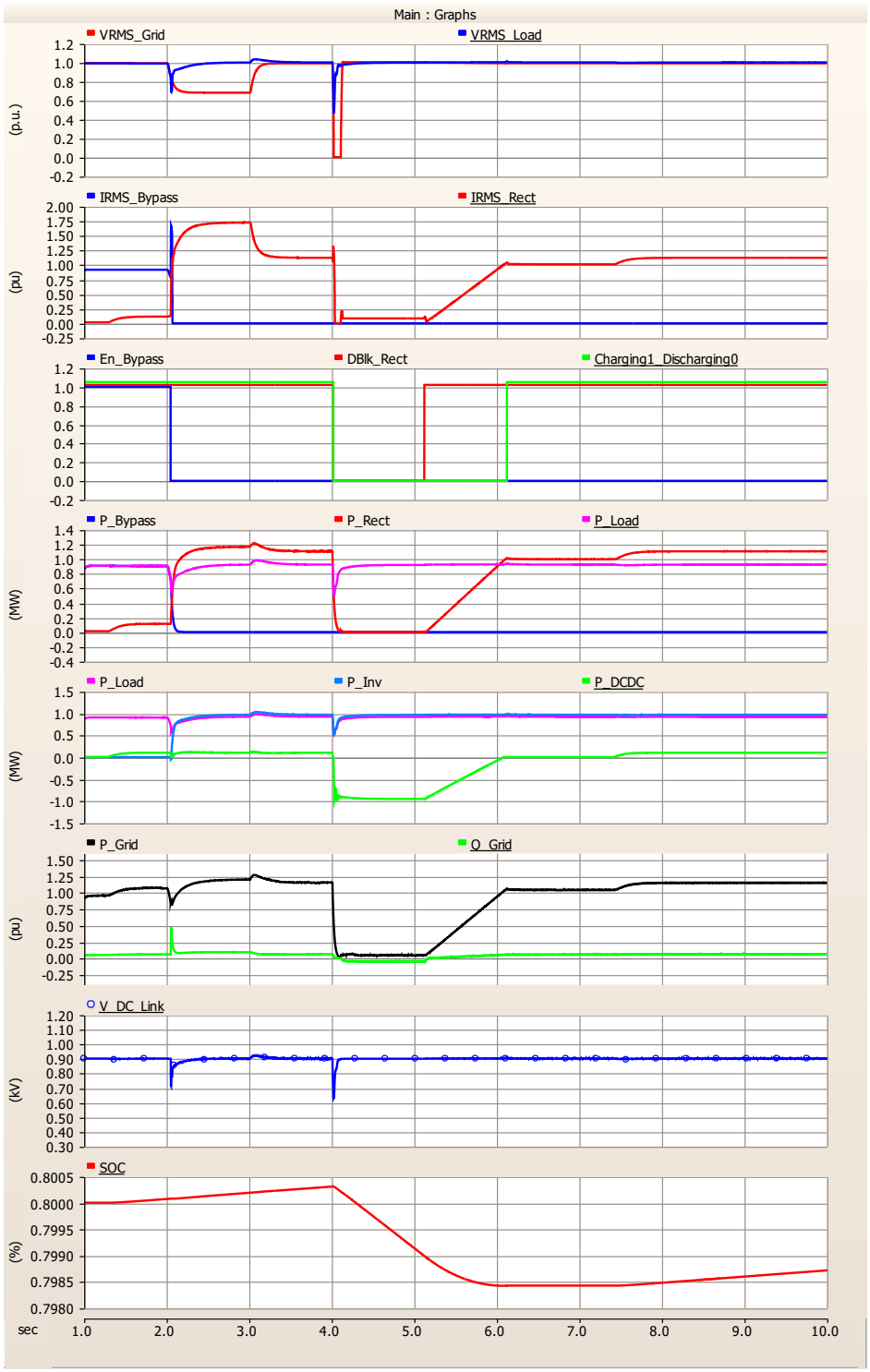


Figure 46: Dynamic result of UPS average model under disturbance (Simulation time step: 50us).

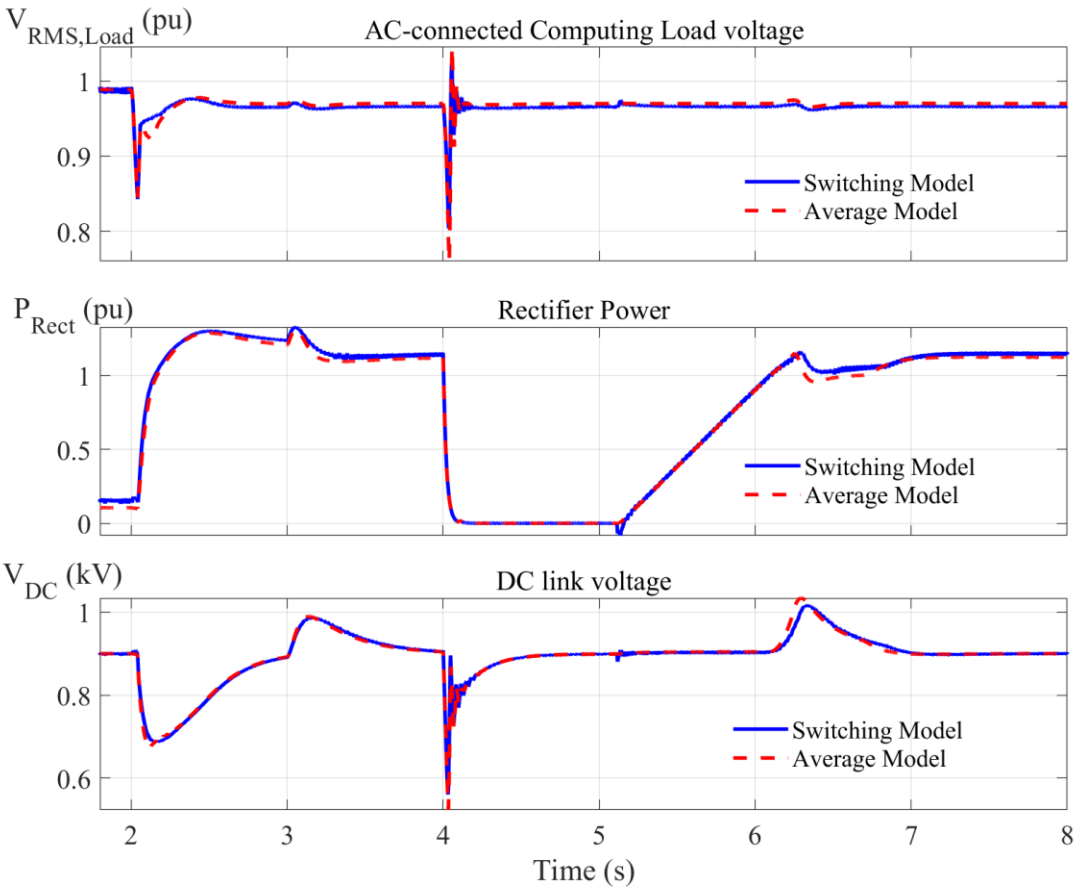


Figure 47: Dynamic performance comparison between the UPS switching model and the average model.

To better compare the dynamic performance of the UPS switching model and the average model, the computing load voltage, rectifier power, and DC-link voltage are extracted and plotted in the same figure. The results are shown in Figure 47, from which it can be observed that their dynamic behaviors are nearly identical.

In addition, for a switching frequency of 10 kHz, a simulation time step of 10 μs is still insufficient to accurately capture the switching-model dynamics. Errors introduced during the switching process can accumulate and manifest as low-frequency oscillations in quantities such as power and DC-link voltage. Figure 48 shows the result of the switching model under a 10us simulation time step. Compared with a 1 us simulation time step in Figure 45, both the power and the DC-link voltage exhibit an additional oscillatory component at approximately 150 Hz. This arises because, with a larger simulation time

step, the high-frequency switching actions cannot be accurately resolved, leading to improper switching transitions.

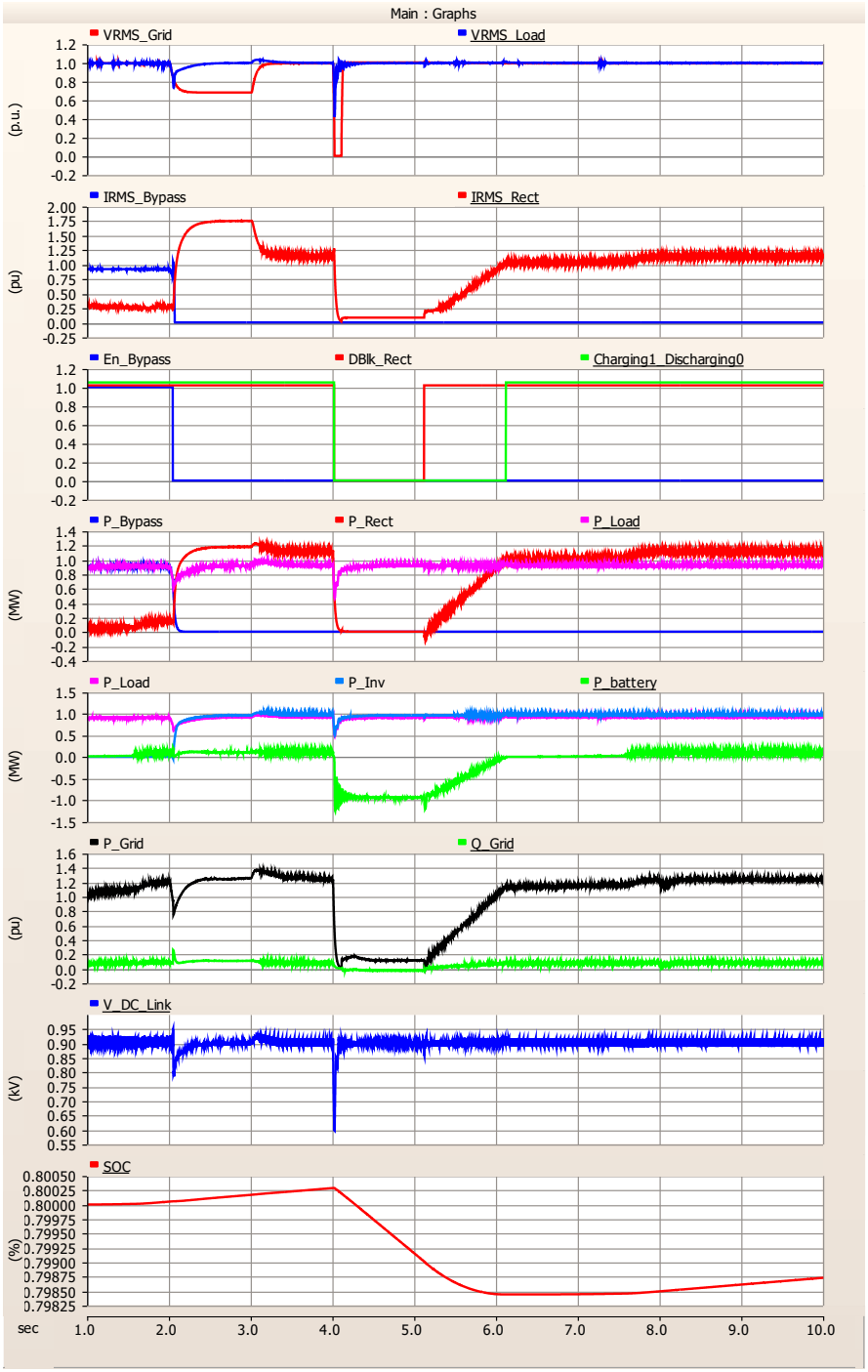


Figure 48: Dynamic performance of switching model (with switch frequency 10kHz and simulation time-step 10us).

Figure 49 and Figure 50 compare the dynamic performance of the VFD motor under the switching model and the average model. “W_m” means the rotational speed of the VFD motor, and “P_VFD” means the input grid power of the VFD. The results show that the responses are highly consistent.

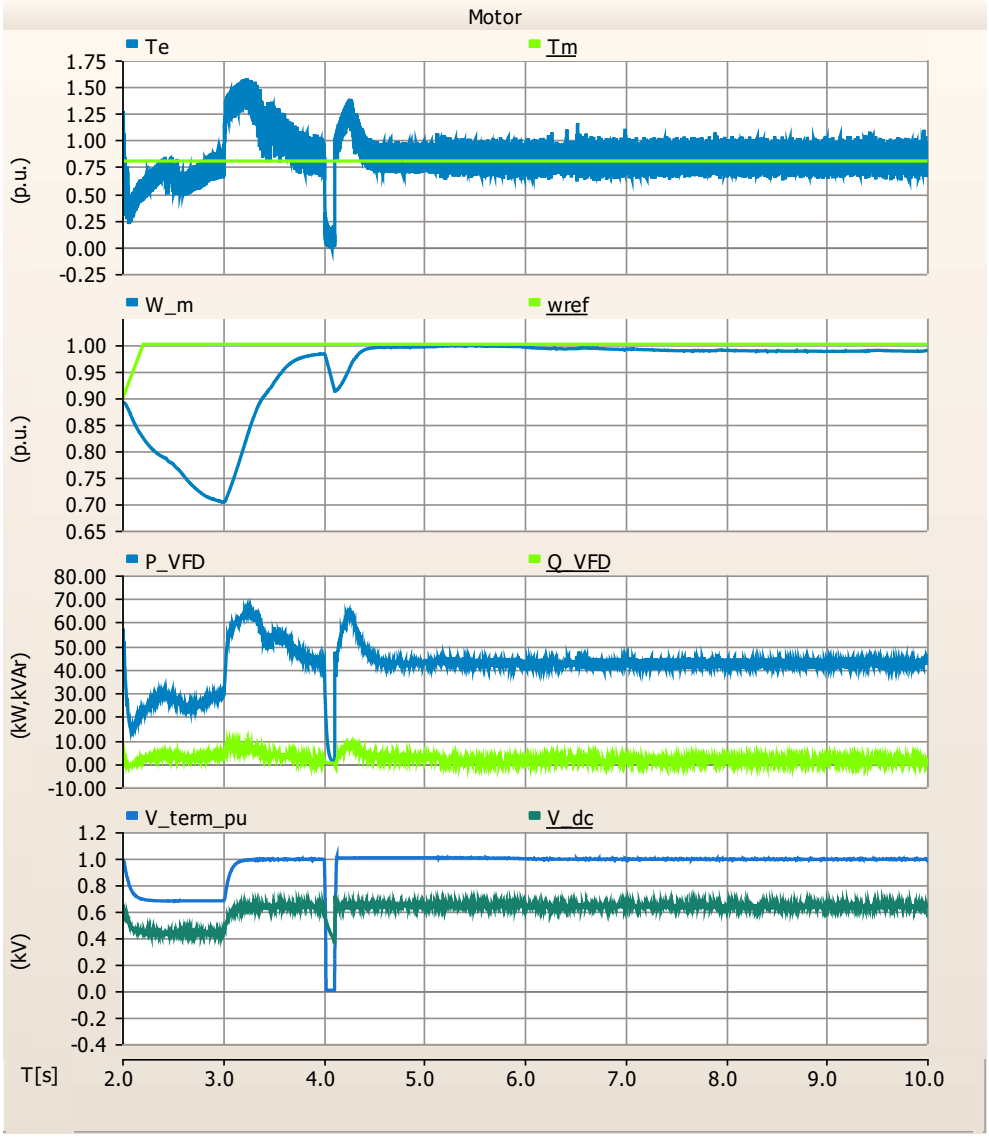


Figure 49: Dynamic result of switching model of VFD under disturbance.

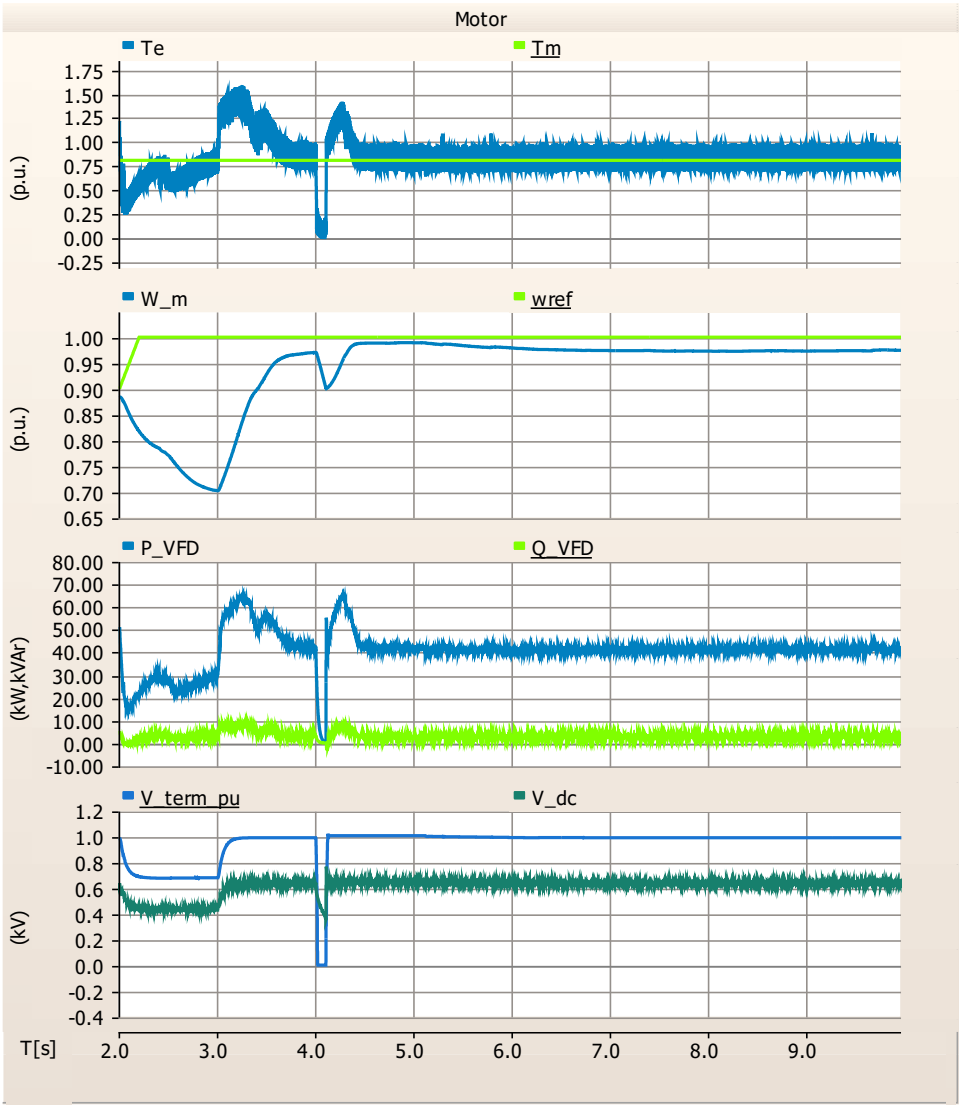


Figure 50: Dynamic result of the average model of VFD under disturbance.

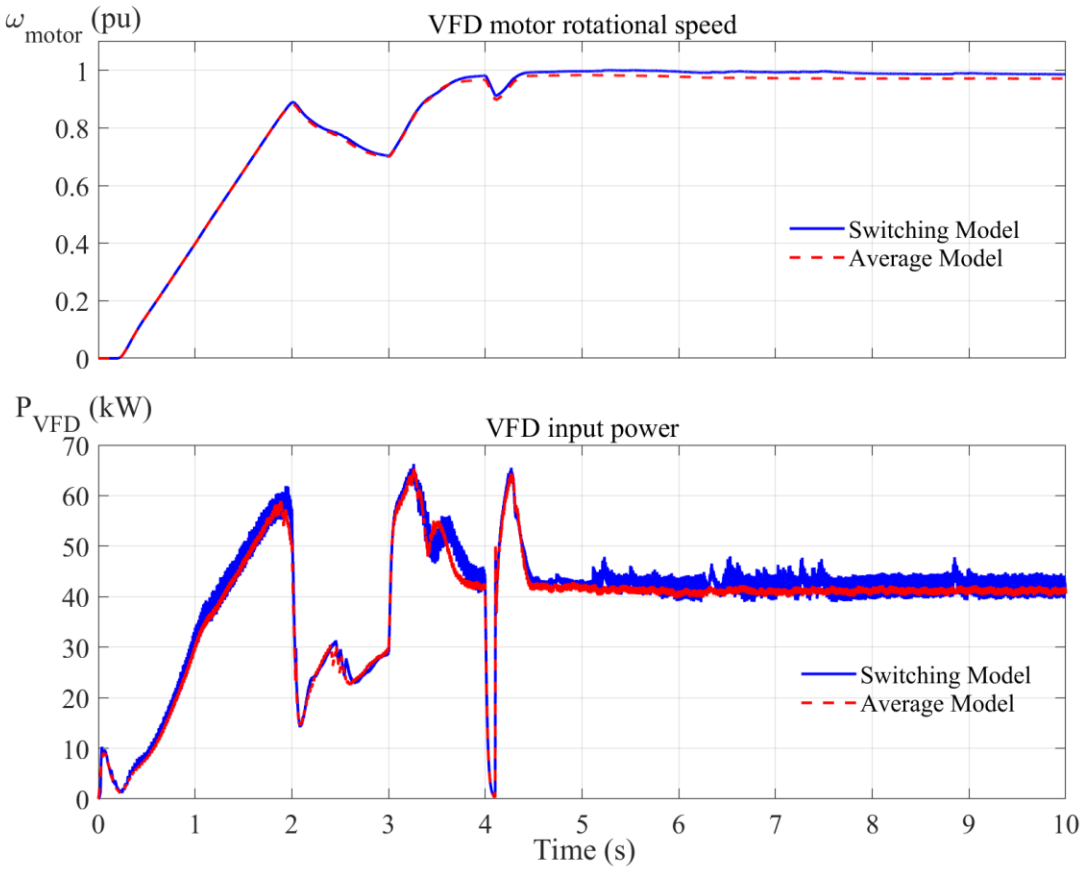


Figure 51: Dynamic performance comparison between the VFD switching model and average model.

For the switching model and the average model of the VFD, the motor speed and instantaneous power are also extracted and plotted in the same figure, as shown in Figure 51, for comparison. The results show that their simulated dynamic responses are nearly identical.

4.4.2. Simulation Efficiency Comparison

Under the same simulation parameters and system scale, the above comparisons demonstrate that the low-frequency dynamic responses of the two models are consistent. Furthermore, their simulation speeds are compared. In the switching model, the switching frequencies of the rectifier, inverter, and the DC/DC converter operate at 10 kHz. The simulations were performed on a system equipped with an AMD Ryzen 9 7950X3D 16-core processor and 128 GB of RAM, and the results are summarized in Table 8.

Table 8: Simulation efficiency comparison between the switching model and the average model.

Simulation time	Simulation timestep	Channel plot step	Simulation time usage of average model	Simulation time usage of switching model
10s	1us	1us	614.219 s (10 min 14 s)	1699.359s (28 min 19s), accurate
10s	10us	10us	48.312 s	450.812 s (7 min 30 s),
10s	20us	20us	26.421 s	396.734 s (6 min 36 s)
10s	50us	100us	15.828s	inaccurate
10s	80us	80us	10.797s	inaccurate

These results demonstrate that the average model significantly improves simulation efficiency while preserving the essential low-frequency dynamic characteristics of the system. Therefore, all subsequent simulations in this report are conducted using the average model.

Furthermore, the impact of the simulation time step is investigated for the average model. It is observed that the simulation remains stable when the time step is smaller than 80 us. For a 10-second simulation with an 80-us time step, the total computation time is only 8.843 seconds. However, when the time step is increased to 100 us, the simulation diverges due to numerical instability. Therefore, a time step of 50 us is recommended for the average model to ensure reliable convergence.

5. UPS Voltage and Frequency Ride-Through Module

This section presents a centralized UPS voltage/frequency ride-through module for coordinated control of the rectifier, inverter, and DC/DC converter during grid disturbances. The ride-through logic and parameter settings are first introduced, followed by the frequency measurement method. Finally, fast and slow reconnection strategies for the rectifier are discussed.

5.1. Ride Through Module

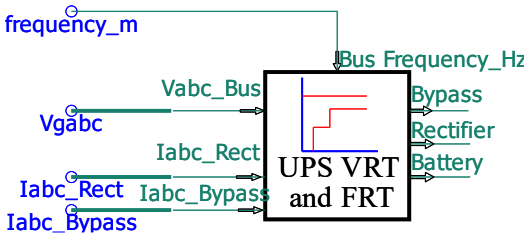


Figure 52: UPS operation mode control and voltage/frequency ride through settings.

The voltage/frequency ride-through module can be viewed as a centralized protection and supervisory control unit within the UPS. As shown in Figure 52, the input signals include the point of common coupling (PCC) voltage and frequency, the AC-side current of the rectifier, and the current flowing through the bypass breaker.

This module continuously monitors the grid voltage, current, and frequency. If any of these quantities exceed predefined thresholds, the bypass breaker is opened to isolate the bypass path. The controller then evaluates the rectifier operating condition. If the rectifier voltage is also abnormal, the rectifier is blocked, allowing the battery to take over the regulation of the DC-link voltage and supply power to the computing load. Once the grid voltage recovers and remains stable for a specified duration, the rectifier is deblocked, the battery ceases discharging, and the UPS returns to normal operation. This coordinated logic ensures uninterrupted load supply while protecting the rectifier and maintaining DC-link stability during grid disturbances.

Other operational rules are summarized as follows:

1) The inverter remains continuously deblocked to guarantee uninterrupted power supply to the load.
2) The battery DC/DC converter also remains deblocked and connected to the DC-link capacitor, operating in either charging or discharging mode depending on the rectifier control state. Specifically, when the rectifier is blocked or during its reconnection phase under active power control, the battery operates in discharging mode to regulate the DC-link voltage.

The voltage/frequency ride-through is based on a comprehensive curve shown in Figure 53, which determines UPS operating mode transitions based on input voltage and frequency conditions.

When the input voltage and frequency remain within the acceptable operating range, the UPS operates in **bypass mode**, supplying the load directly from the bypass line. If the voltage or frequency deviates beyond allowable limits, the UPS transitions to **normal converter mode**, in which the load is supplied through the rectifier and inverter. For more severe deviations, the UPS transitions to **battery backup mode**, when the rectifier is tripped from the grid and the battery discharges to maintain the DC-link voltage and supply power to the load. Once the input voltage and frequency recover to the acceptable ranges, the system transitions back to normal converter mode.

The stepped voltage and frequency boundaries define the thresholds for mode transitions, providing protection against abnormal grid conditions.

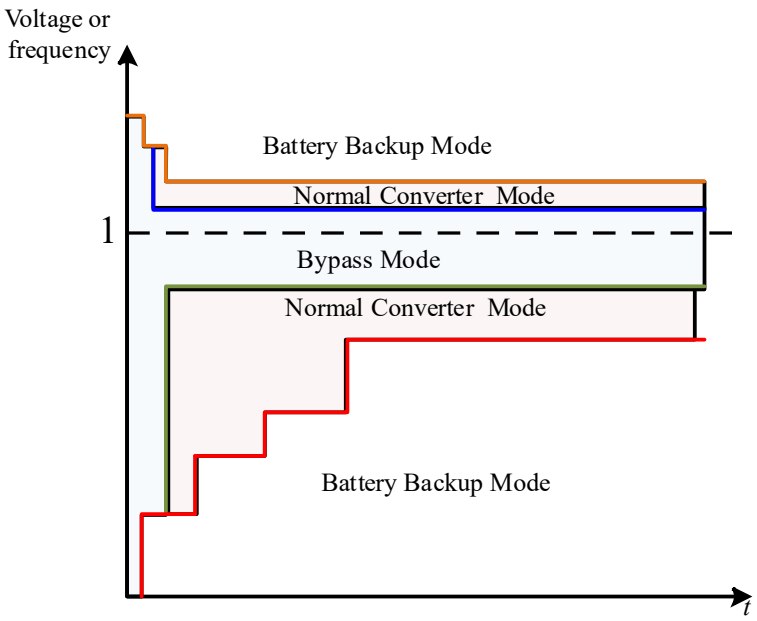


Figure 53: Voltage/frequency ride-through curve of UPS.

An overcurrent protection curve can also be defined, as shown in Figure 54, which specifies both the threshold and the associated hold-up time.

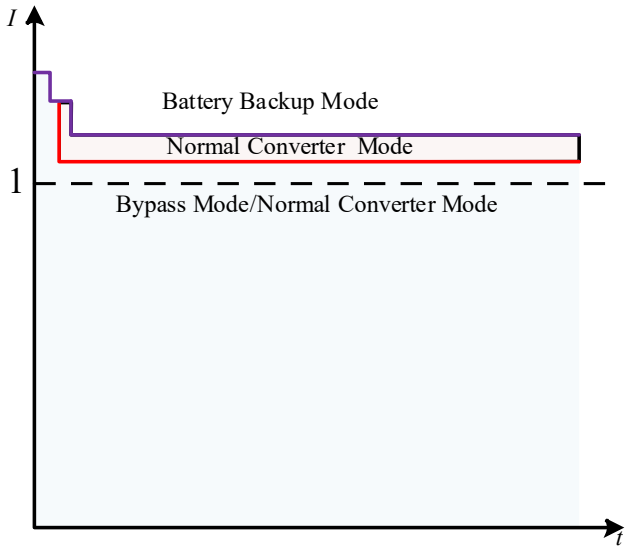


Figure 54: Overcurrent ride through curve.

5.2. VRT Parameters Settings

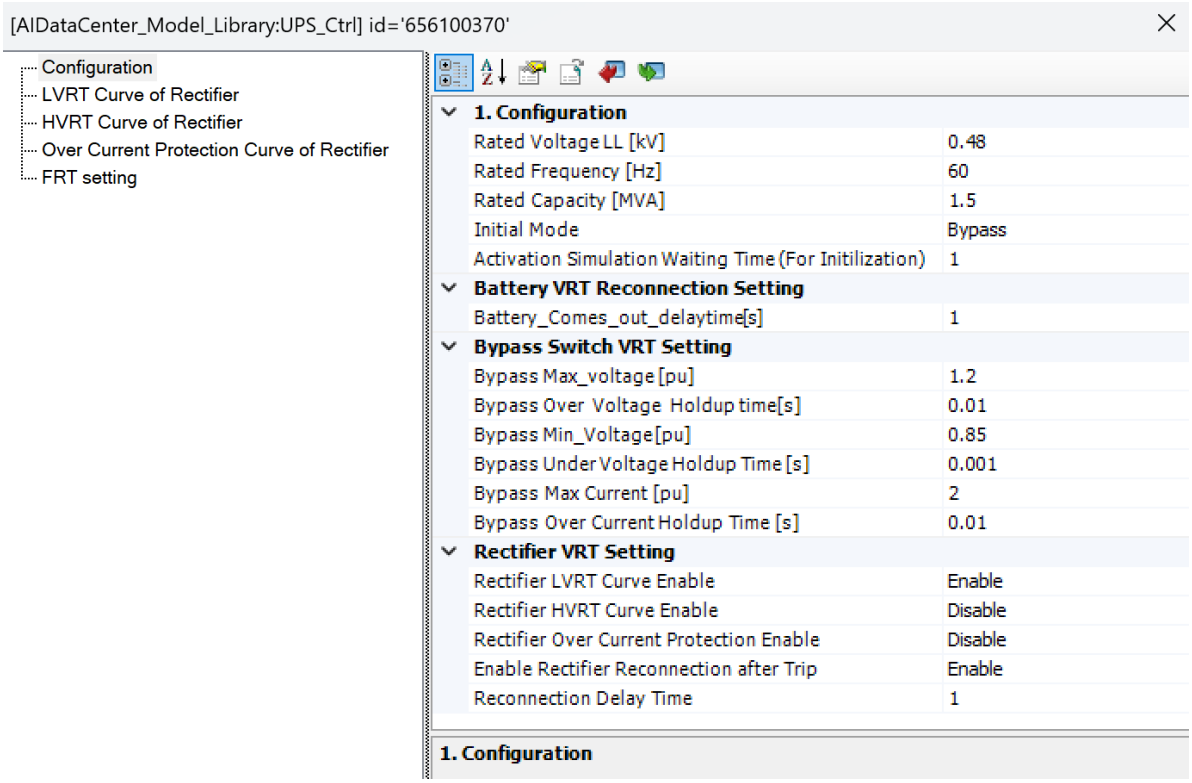


Figure 55: Protection parameters of UPS.

The protection system parameters are shown in Figure 55, presents the configuration interface of the UPS control block used in the model. The controller allows users to specify rated system parameters, including voltage, frequency, and power capacity, as well as the initial operating mode.

In addition, the bypass switch voltage ride-through (VRT) settings can be configured, including the allowable voltage range, hold-up times for overvoltage and undervoltage conditions, and the maximum permissible current during bypass operation.

The controller also provides configurable rectifier protection and ride-through settings, including the enabling or disabling of low voltage ride-through (LVRT) and high voltage ride-through (HVRT) characteristics, overcurrent protection, and rectifier reconnection following a trip. These parameters enable the UPS control behavior to be adapted to different grid conditions and operational requirements.

For rectifier LVRT, HVRT, and overcurrent protection, the characteristics can be defined using multi-point curves rather than a single threshold. Figure 56 illustrates the configuration interface of the rectifier LVRT curve in the UPS control model. The LVRT characteristic is defined by a set of RMS voltage thresholds and corresponding hold-up times. The RMS voltage points determine the voltage levels at which ride-through performance is evaluated, while the hold-up times specify the duration for which the rectifier is allowed to remain connected under each voltage condition.

By adjusting these parameters, users can define the voltage ride-through capability of the rectifier, allowing the UPS to either sustain operation during short-duration voltage dips or trip when the voltage remains below specified thresholds for longer periods. If a particular point is not intended to be active, its hold-up time can be set to 999.

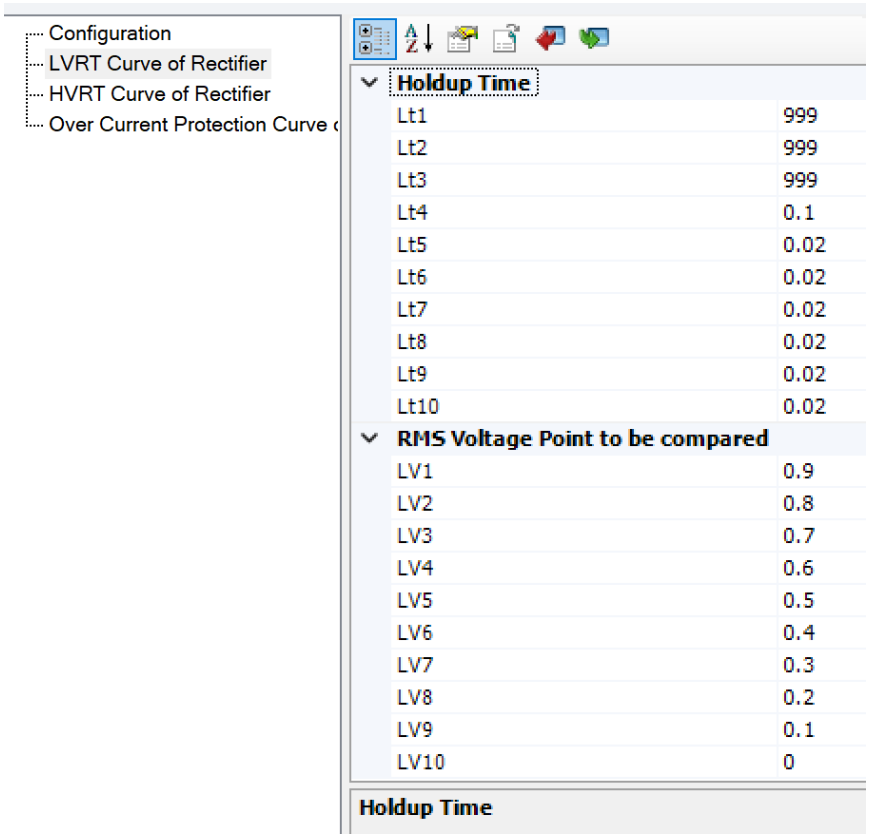


Figure 56: LVRT curve of rectifier.

5.3. FRT Parameters Settings

High- and low- frequency ride-through settings are also configured in the model, as shown in Figure 57. These parameters include the upper and lower frequency thresholds, as well as the corresponding hold-up times for both the bypass switch and the rectifier. The frequency ride-through logic follows a structure similar to that of the voltage ride-through.

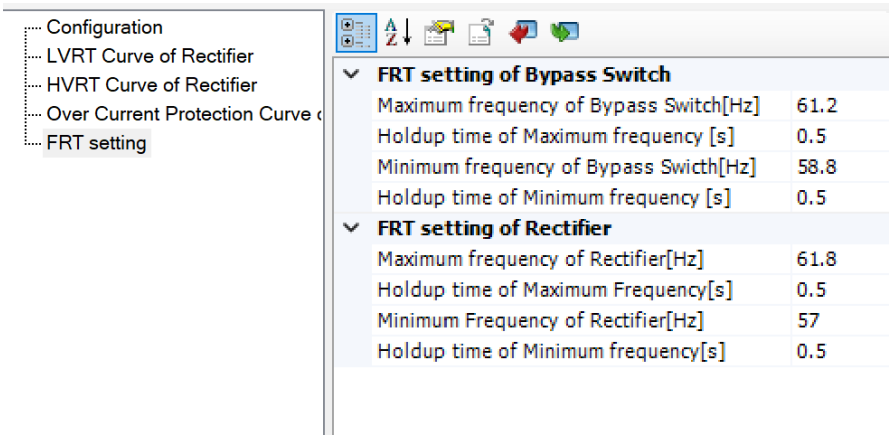


Figure 57: Frequency ride-through parameters.

The frequency measurement from the Rectifier PLL is employed to measure bus frequency with a low-pass filter, as illustrated in Figure 58:

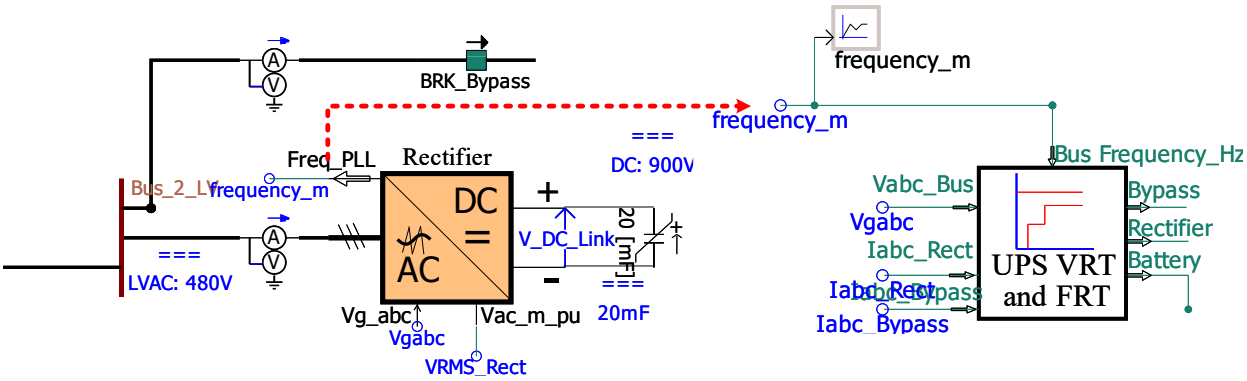


Figure 58: Frequency measurement for FRT control.

5.4. Fast and Slow Reconnection of Rectifier

Following a fault, the rectifier reconnection delay is defined as shown in Figure 59. Two reconnection strategies are considered.

The first one is **fast reconnection**, in which the delay is very short (typically less than 1 s, and often on the order of 0.1–0.2 s). For such brief interruptions, the ramp rate can be set relatively high, since the grid frequency does not change significantly during this period.

The second option is **slow reconnection**, where the rectifier remains disconnected for a longer duration (ranging from several seconds to minutes). In this case, the grid frequency may have already increased due to the large load disconnection. Therefore, a smaller ramp rate is required to ensure a stable and smooth reconnection process.

During the reconnection process, the rectifier power is subject to ramp-rate limitations. The rectifier operates in active power control mode and gradually increases its output toward the reference value according to the specified ramp rate. Meanwhile, the battery maintains the DC-link voltage until the rectifier fully restores its power output.
The recovery time can be estimated as:

$$t_{\text{reconnection}} = \frac{P_{\text{load}}}{R_{\text{ramp}}}, \tag{5.1}$$

where P_{load} is the computing load demand and R_{ramp} is the rectifier power ramp rate.

Accordingly, a parameter referred to as the battery come-out delay time is introduced. This delay is set equal to $r_{\text{reconnection}}$.

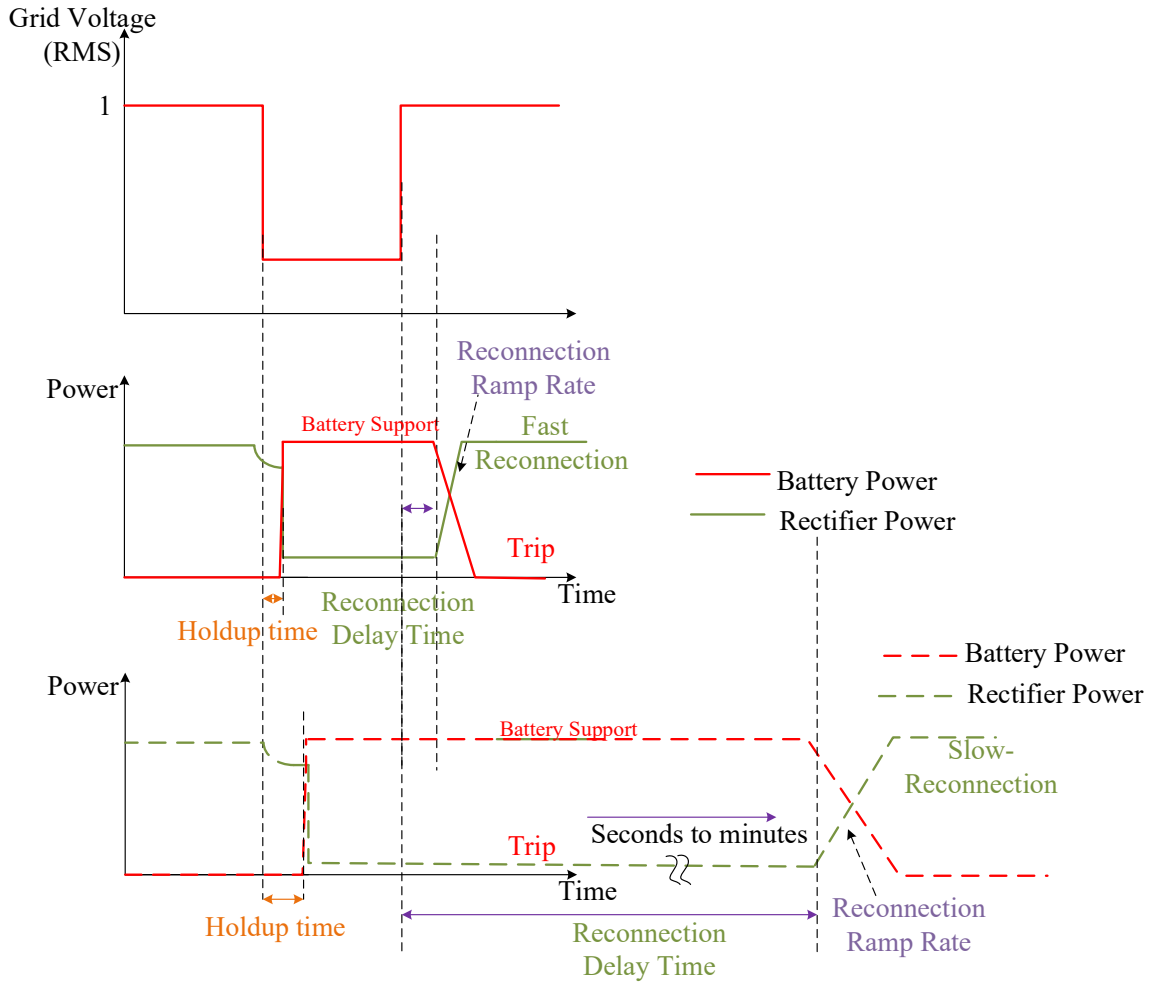


Figure 59: Time-series illustration of AI data center load tripping and subsequent reconnection, comparing fast and slow reconnection scenarios.

6. Double-Conversion UPS-Based AI Data Center Model

Building on the modular models described above, this section presents the complete double-conversion UPS-based AI data center model and evaluates its dynamic performance under different operating scenarios. The electrical topology and operation modes are first introduced, followed by studies on UPS voltage ride-through and mode transitions during grid disturbances. Load reconnection dynamics and representative test cases are then examined. Finally, the variable computing loads are tested and the power fluctuations in AI data center are demonstrated.

6.1. Electrical Topology

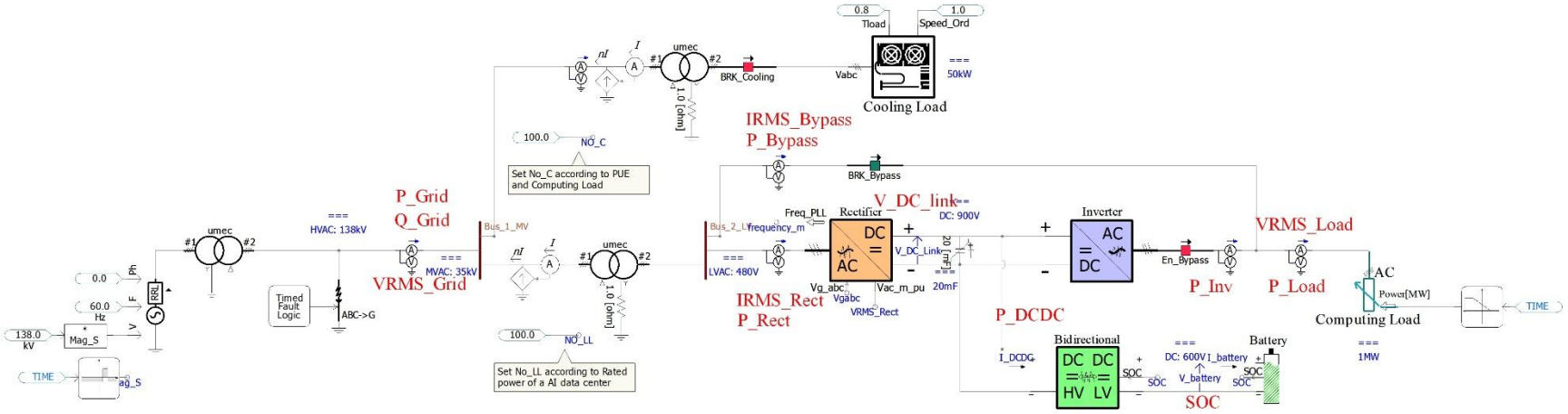


Figure 60: Double-conversion UPS-based AI data center model in PSCAD.

Figure 60 illustrates the overall system model of the AI data center power supply based on a double-conversion UPS architecture. The grid supplies power through a transformer and distribution network to the data center load. The UPS system consists of an AC/DC rectifier, a DC link capacitor, a DC/AC inverter, and a battery energy storage system interfaced through a bidirectional DC/DC converter. Under normal operating conditions, the rectifier supplies the DC link, and the inverter delivers regulated AC power to the load. During grid disturbances, the battery supports the DC link to maintain uninterrupted power supply.

The rated parameters of the rectifier, inverter, bidirectional DC/DC converter, computing load, and cooling load are summarized in Table 9.

Table 9: Rated Parameters for UPS.

Converter Model	Rated power	Rated AC voltage(L-L)	Rated DC voltage	Saturated Current
Rectifier	1.5 MVA	480V	900V	1.3 pu (1.95pu in 1 MVA base)
Inverter	1MVA	480V	900V	1.5 pu
DC/DC converter	1MVA	-	900V	-
Computing Load	1MW	480V	-	-
VFD cooling load	0.05MVA	480V	-	-

To represent a large-scale AI data center, a current scaling approach is applied in the model. Specifically, a current scaler is used to scale up the UPS capacity from a **1 MW** base model to an equivalent **100 MW** system. Similarly, the cooling load is scaled from a base value of **50 kW** to **12.5 MW** to capture the aggregated cooling demand in a large data center.

This scaling approach enables the use of a detailed UPS model while representing large system power levels. Users can adjust these parameters according to the actual capacity and power usage effectiveness (PUE) of a specific AI data center.

6.2. Operation Modes

The operations of the AI data center can be classified into three modes: **bypass mode**, **normal converter mode**, and **battery backup mode**.

6.2.1. Bypass Mode

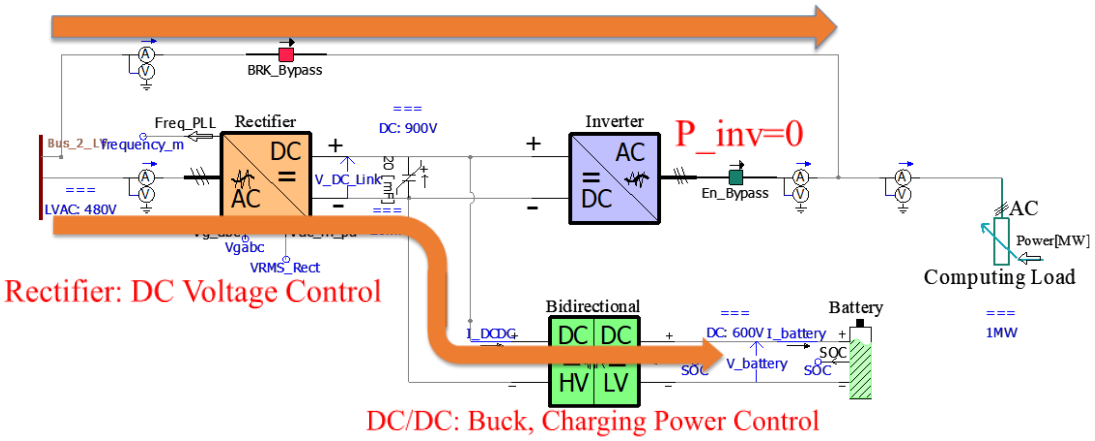


Figure 61: Bypass mode of the AI data center operation.

In bypass mode, the AI data center load is supplied directly by the utility grid, bypassing the UPS inverter stage. As illustrated in Figure 61, the grid voltage is stepped down through transformers and delivered to the data center distribution bus, which supplies both computing loads and cooling systems. In this mode, the rectifier and inverter do not participate in load supply, while the battery energy storage system remains in standby or charging mode.

6.2.2. Normal Converter Mode

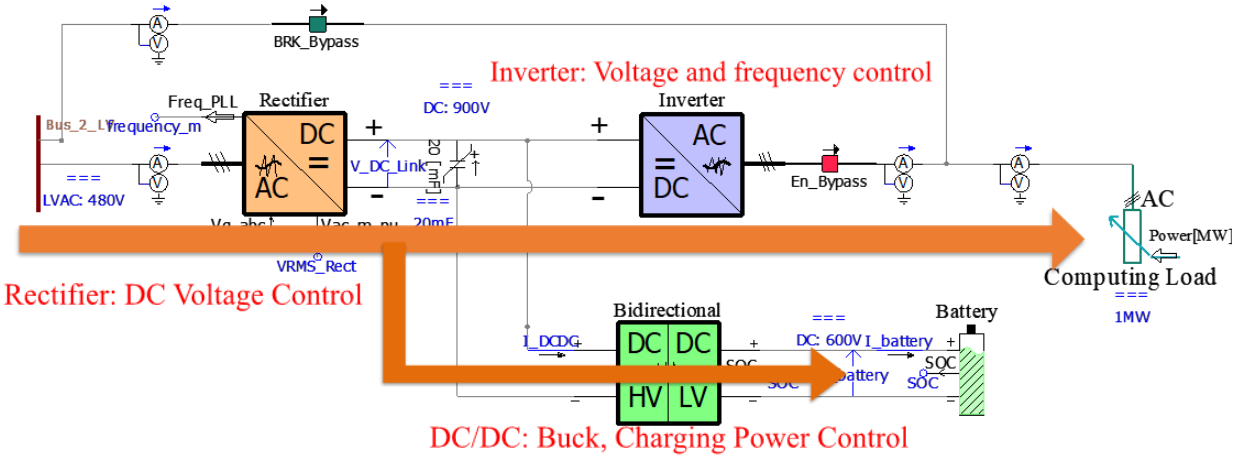


Figure 62: Normal converter mode of the AI data center operation.

In normal converter mode, the AI data center is supplied through the UPS conversion system, which provides power conditioning and ensures stable operation of the computing loads. As shown in Figure 62, the AC grid power is first converted to DC by the AC/DC rectifier, which operates in grid-following mode and regulates the DC-link voltage. By maintaining a stable DC bus voltage, the rectifier ensures that sufficient energy is available for the downstream converters.

The DC/AC inverter operates in grid-forming mode with AC voltage and frequency control, generating a stable AC voltage and frequency for the data center distribution bus. In this configuration, the inverter behaves as a controlled voltage source and supplies the computing loads with regulated voltage and frequency, effectively isolating critical loads from upstream grid disturbances.

Meanwhile, the battery energy storage system is interfaced through a DC/DC converter operating in buck mode. Under normal conditions, this converter typically operates in charging power control mode, allowing the battery to absorb energy from the DC link and maintain the desired state of charge.

6.2.3. Battery Backup Mode

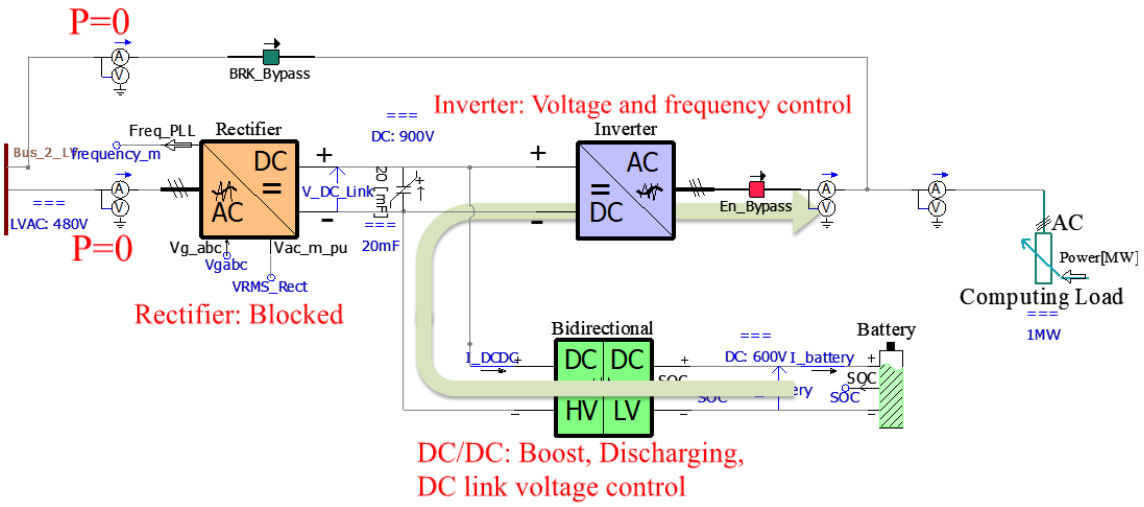


Figure 63: Battery backup mode of the AI data center operation.

In battery backup mode, the AI data center continues operating when the upstream grid supply is unavailable. As illustrated in Figure 63, the AC/DC rectifier is no longer able to regulate the DC-link voltage, and the battery energy storage system becomes the primary energy source.

The DC/DC converter operates in boost mode, drawing energy from the battery and regulating the DC-link voltage. By maintaining a stable DC link, it ensures that the inverter has a reliable energy source to supply the loads.

The DC/AC inverter operates in grid-forming mode with voltage and frequency control, generating the required AC voltage and frequency for the data center. In this mode, the inverter establishes the electrical reference for the local AC system, enabling islanded operation supported by the battery.

During battery backup operation, the energy stored in the battery is gradually depleted to sustain the load. The DC/DC converter maintains DC-link stability, ensuring continuous and reliable operation of the computing loads until grid power is restored or alternative backup generators become available.

6.3. UPS Voltage Ride-Through and Mode Transition

In this section, the dynamic performance of voltage ride-through and the system behavior during mode transitions are presented. All results are based on the average model. The definition of the variable name in the result can be found in Figure 60.

6.3.1. Grid Voltage Sag and Mode Transition

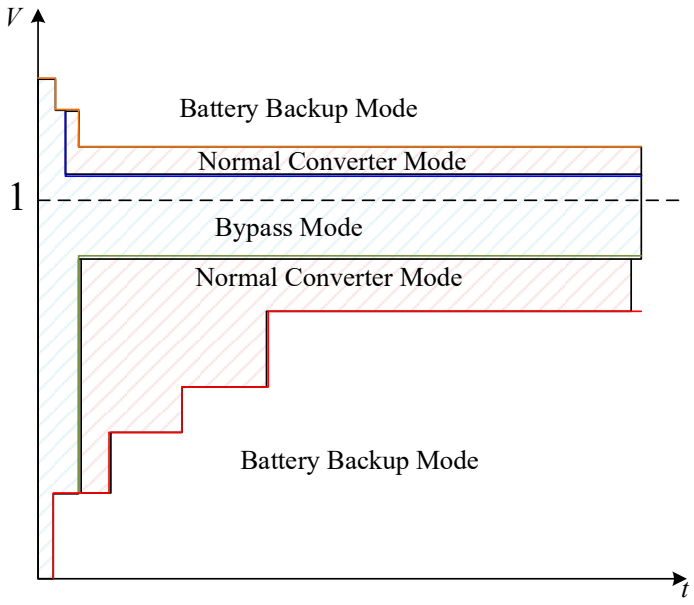


Figure 64: Mode transition during voltage sag.

When a grid voltage or frequency disturbance occurs, the UPS may transition from bypass mode to normal converter mode and subsequently to battery backup mode, as shown in Figure 64. To define the mode transition, the voltage, frequency, and current protection parameters can be configured within the protection module described in Section 5. In addition, the VRT curve can be specified, and the model automatically initiates tripping according to the defined curve.

Two case studies are presented below to illustrate the dynamic response during voltage sag events. The corresponding UPS VRT protection settings are shown in Figure 65. For the VRT curve configuration, a single-point characteristic is used for both the bypass

breaker and the rectifier in this example. These settings can be readily modified to accommodate more general multi-point VRT curves as required.

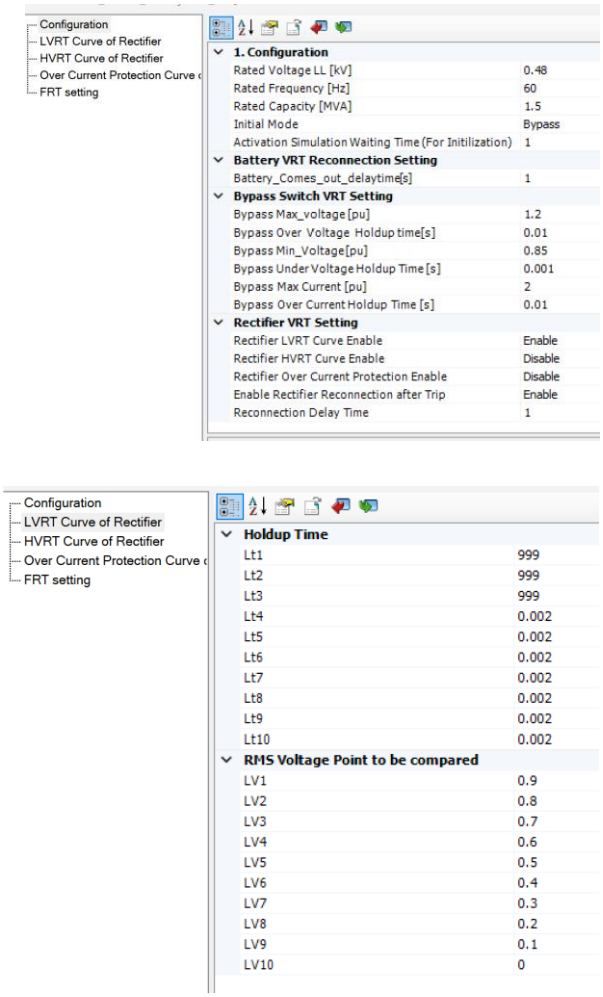


Figure 65: Parameter settings for voltage sag and mode transition.

1) From Bypass Mode to Normal Converter Mode (voltage drop from 1 to 0.7 pu)

Before t = 4s, UPS operates in bypass mode. The IT computing load is 1MW, and the battery is in charging mode with a charging power of 0.1 MW.

At t = 4s, grid voltage sags to 0.7 pu. Since the minimum voltage threshold of the bypass breaker is set to 0.85 pu with a hold-up time of 1 ms, the UPS transitions from bypass mode to normal converter mode. The dynamic responses of RMS voltage (grid-side PCC voltage and load-side inverter output voltage), current, active and reactive power, and state of charge (SOC) are shown in Figure 66.

The first subplot in Figure 66 shows the grid-side voltage and the load-side voltage (i.e., the voltage at the IT load). In this configuration, the inverter is not synchronized with the grid during bypass operation. Instead, a switch is installed at the inverter output and is coordinated with the bypass breaker. This switch is closed only after the bypass breaker opens. It can be observed that when the grid voltage drops to 0.7 pu, the inverter rapidly takes over the load, and the minimum load voltage remains around 0.85 pu.

The second subplot shows the currents of the inverter and the bypass breaker. After the bypass breaker trips, the inverter current increases. Due to the reduced grid voltage, the inverter current exceeds its nominal value. In addition, the rectifier must recharge the DC-link capacitor, resulting in a short-duration overcurrent limited by the current limiter. As the DC-link voltage recovers, the rectifier current gradually decreases.

The third subplot presents the enable signals of the bypass breaker, rectifier, battery, and inverter. The green curve indicates the battery operating mode (1 for charging and 0 for discharging). In bypass mode, the bypass breaker is closed, the rectifier is enabled to charge the battery.

The fourth subplot shows the power through the bypass breaker, the rectifier power, and the load power. When the system transitions from bypass mode to normal converter mode, the computing load power remains nearly constant despite the voltage sag.

The fifth subplot illustrates the computing load power, inverter output power, and battery power (i.e., DC/DC converter power, where positive values indicate charging and negative values indicate discharging). During the voltage sag, the inverter power rapidly increases to supply the computing load.

The sixth subplot shows the grid-side active and reactive power. The total grid power is the sum of the bypass breaker power and the rectifier power. Following the voltage sag, the grid power initially decreases, then exhibits an overshoot, and finally settles. The initial decrease is due to the voltage drop and bypass disconnection, while the subsequent

increase occurs as the rectifier ramps up to supply both the load and the DC-link energy. Once the DC-link voltage is restored, the rectifier power balances the inverter (load) power and battery power.

The seventh and eighth subplots show the DC-link voltage and battery SOC, respectively. At the onset of the voltage sag, the computing load behaves approximately as a constant power load due to the inverter voltage regulation. The rectifier requires time to restore the DC-link voltage. When the DC-link voltage drops below a certain level, battery charging is temporarily interrupted. After the DC-link voltage recovers, the battery resumes charging.

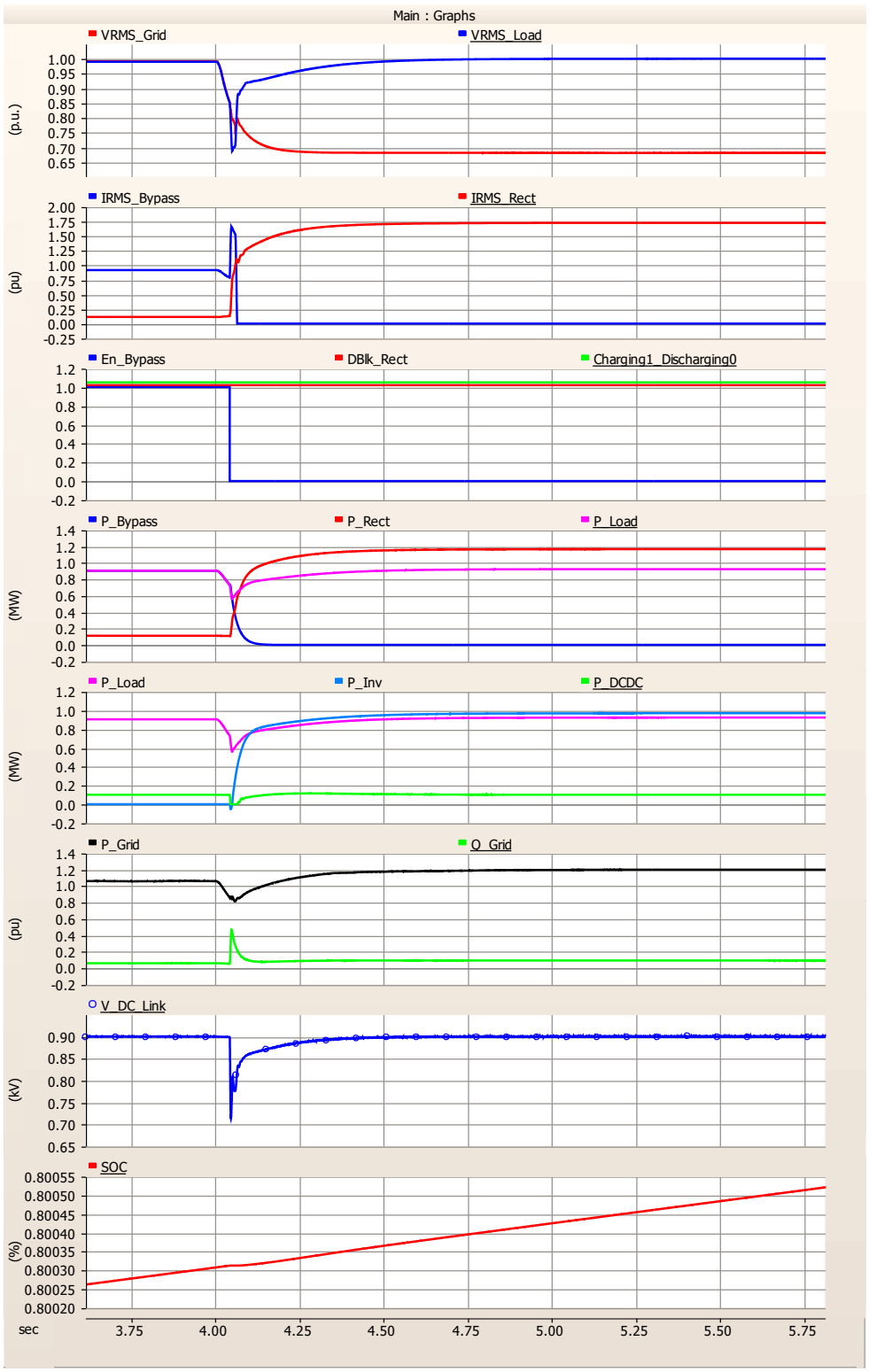


Figure 66: Dynamic results when UPS transitions from bypass mode (t < 4.02s, inverter is not synchronized with grid) to normal converter mode (t > 4.02s). Refer to Figure 60 for the variable name definitions.

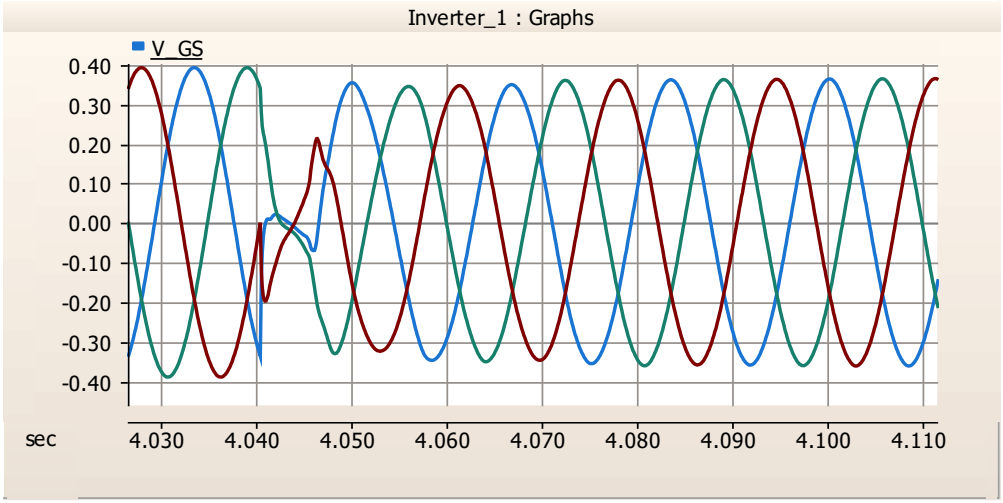


Figure 67: Instantaneous inverter output AC voltage during a grid voltage sag and bypass breaker trip.

Figure 67 shows the instantaneous AC voltage at the inverter output terminal connected to the IT computing load at the moment of the grid voltage sag. It can be observed that the voltage is generally maintained constant, with only a transient variation in magnitude.

2) **From normal converter mode to battery backup mode (voltage drop from 0.7 to 0.5 pu)**

Figure 68 presents the dynamic response when the grid voltage decreases from 0.7 pu to 0.5 pu, triggering a transition from normal converter mode to battery backup mode. The rectifier trips when the grid voltage falls below 0.6 pu for 2 ms. Following the rectifier trip, the grid-side power drops to zero.

The battery then rapidly takes over DC-link voltage regulation, transitioning from charging to discharging mode and restoring the DC-link voltage. During this process, the computing load voltage remains nearly constant, with a minimum value of approximately 0.9 pu, and the load power is also maintained with minimal variation.

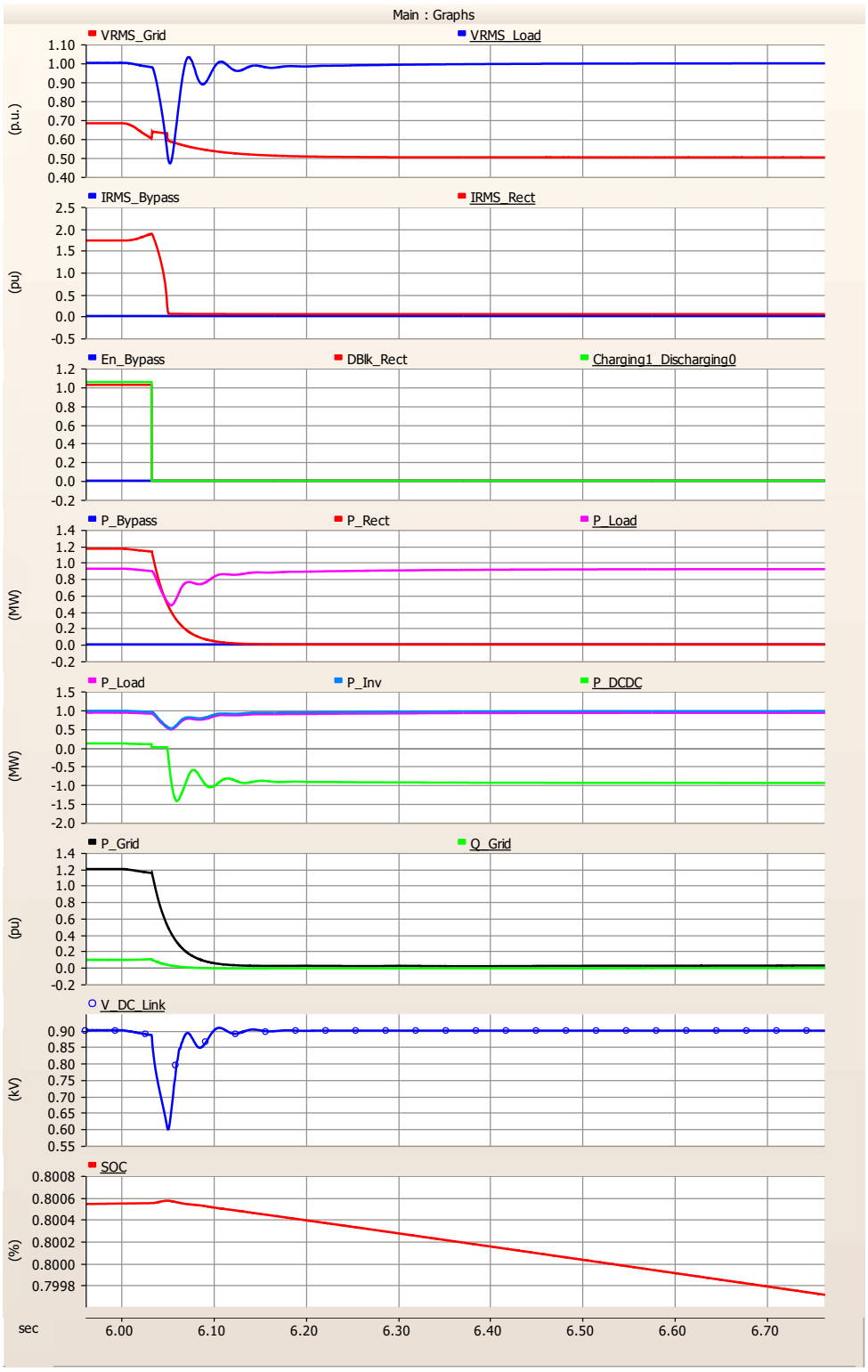


Figure 68: Dynamic results when UPS transitions from normal converter mode (before t = 6.04s) to battery backup mode (t>6.04s). Refer to Figure 60 for the variable name definitions.

6.3.2. AI Data Center Load Reconnection

6.3.2.1. Fast and Slow Reconnection

The previous cases focused on voltage sag events and the corresponding mode transitions. In this section, the reconnection dynamics of data center loads after grid recovery are investigated.

The tripping and reconnection of large data center loads are critical to grid stability. With battery support, rectifier power can be reduced during a grid voltage sag and restored immediately after voltage recovery, a strategy referred to as **fast reconnection**. Fast reconnection is generally feasible when the voltage sag is brief and recovery is rapid, resulting in minimal impact on grid frequency and supporting overall system stability. However, when the voltage sag persists for a longer duration, grid frequency and the power balance may already have changed. In such cases, fast reconnection may adversely affect system stability, and a **slow reconnection** strategy, in which the data center load is gradually restored, may be more appropriate.

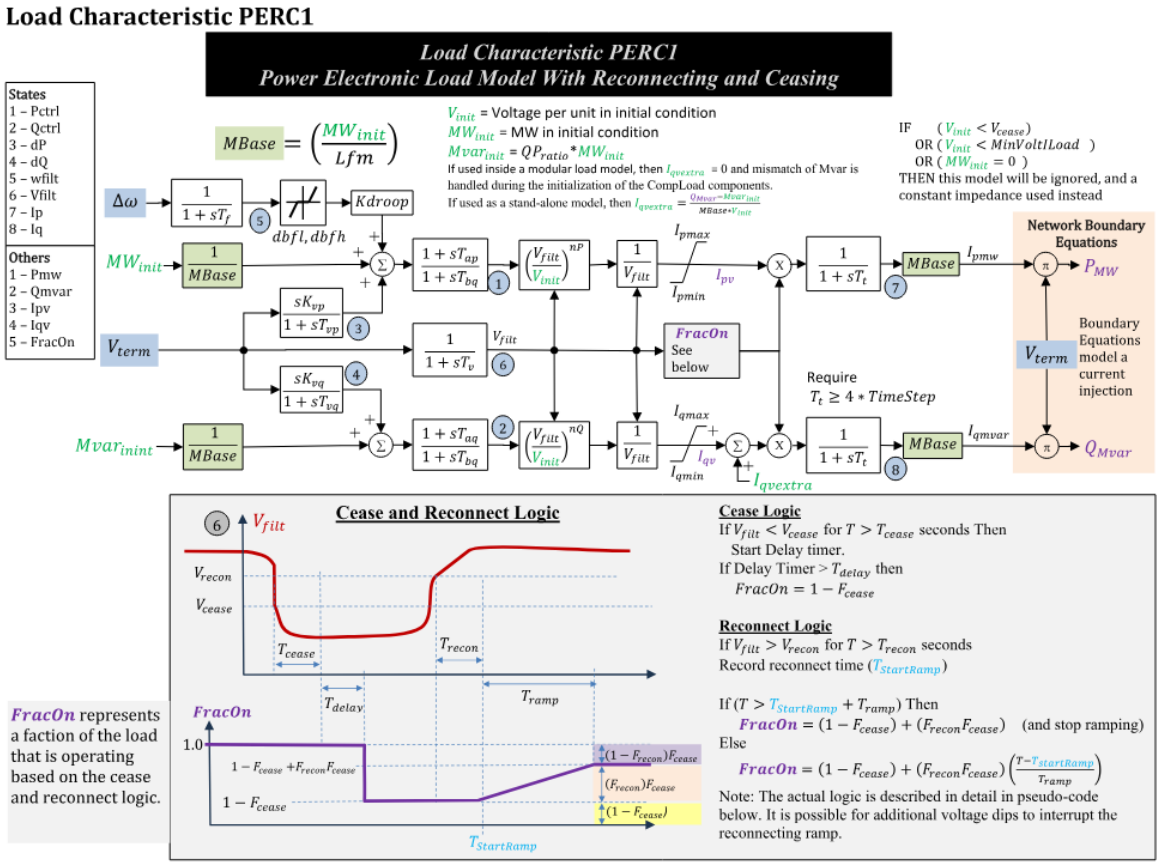


Figure 69: PERC1 model in PowerWorld.

PowerWorld provides a sequential control logic model, PERC1, for modeling the tripping and reconnection of power-electronic loads [16], as illustrated in Figure 69. Similar time-sequence logic is adopted in commercial UPS system [17]. For example, Schneider Electric defines two rectifier reconnection strategies, namely the traditional UPS scheme and the updated UPS scheme, as shown in Figure 70.

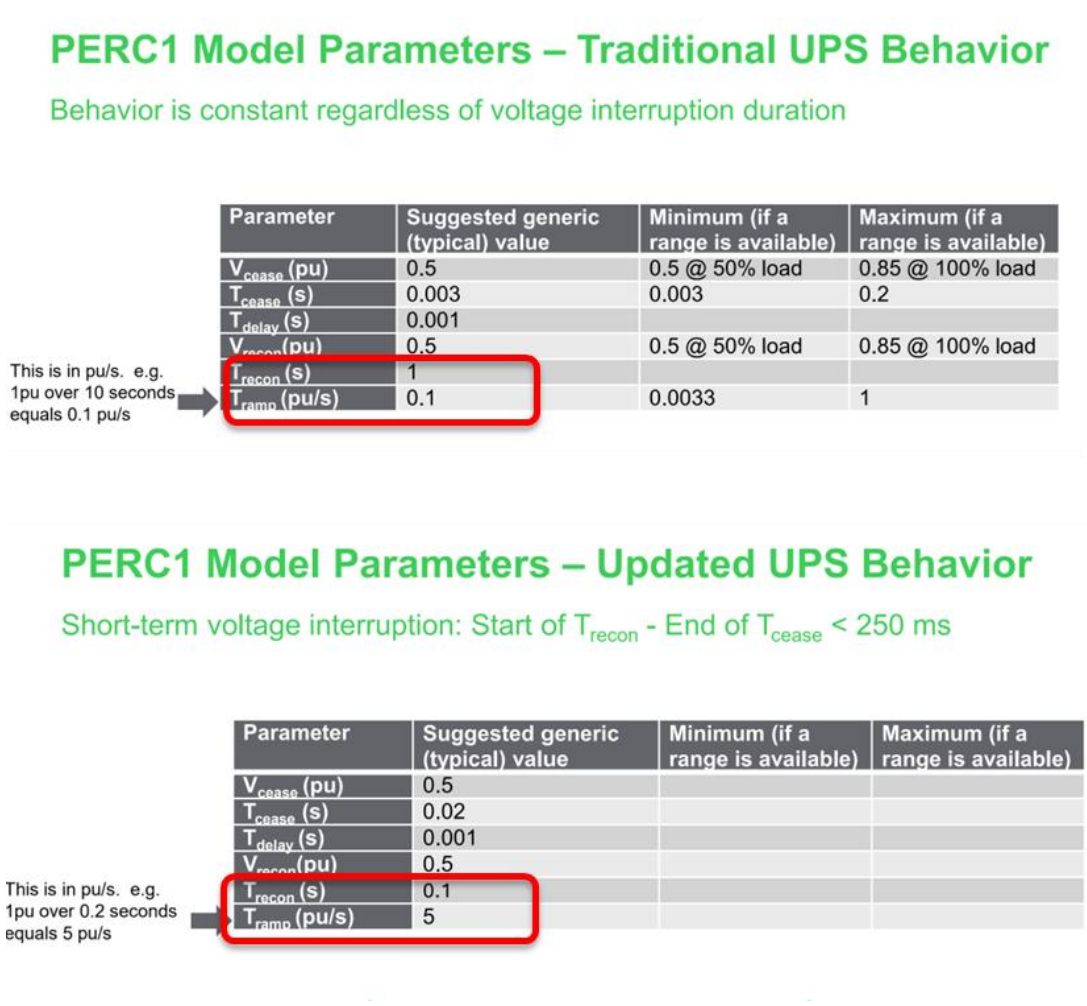


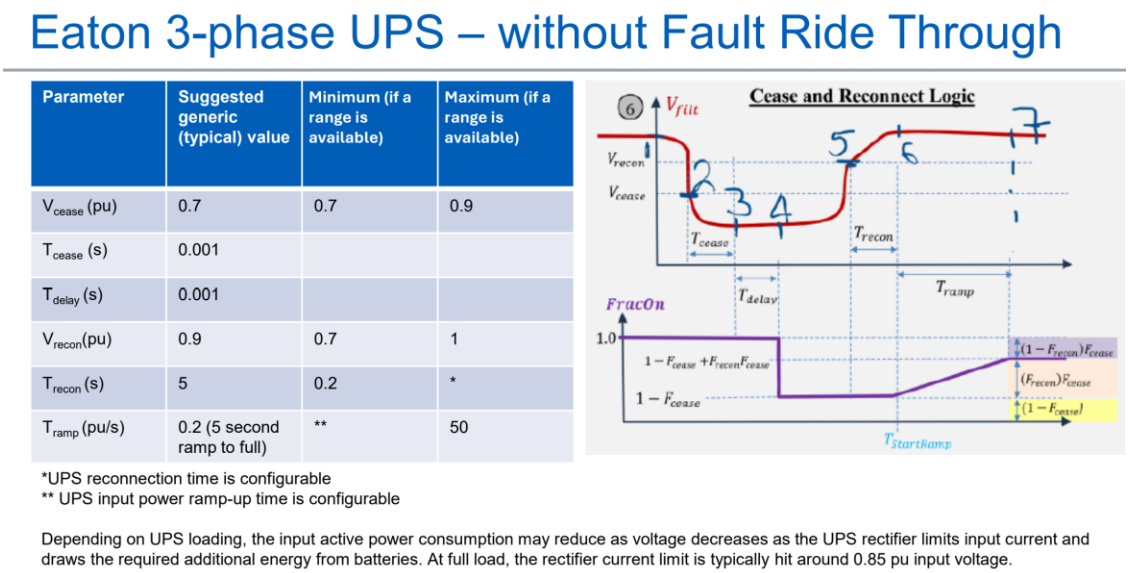
Figure 70: Two types of UPS ceasing and reconnection model given by Schneider.

In the traditional scheme, the reconnection delay is 1s and the post-reconnection power ramp rate is limited to 0.1 pu/s. As a result, it takes approximately 10 s for the load power to fully recover. This behavior corresponds to the **slow reconnection** defined in this report.

In the updated scheme, the reconnection delay is reduced to 0.1 s. Since the grid frequency has not yet significantly responded, the load power can be restored much more rapidly, with ramp rates up to 5 pu/s. Consequently, the total recovery time is approximately 0.3 s. This behavior corresponds to the **fast reconnection** defined in this report.

Similarly, Eaton Corporation provides traditional and updated three-phase UPS models, as shown in Figure 71 and Figure 72, corresponding to slow and fast reconnection, respectively. In the updated design, the reconnection delay is reduced from 5 s to 0.2 s, while the allowable ramp rate increases from 0.2 pu/s to 20 pu/s.

It should be noted that the load ramp rate must be selected in accordance with the reconnection delay, as the grid frequency response depends on the duration of the interruption. After a long disconnection, reconnection should be treated as a new startup, and the ramp rate should be limited to avoid large frequency deviations. In contrast, when the disconnection is short and reconnection occurs rapidly, the ramp rate limits may be relaxed, and fast power restoration can further support overall grid stability.



Eaton 3-phase UPS – without Fault Ride Through

Parameter	Suggested generic (typical) value	Minimum (if a range is available)	Maximum (if a range is available)
V_{cease} (pu)	0.7	0.7	0.9
T_{cease} (s)	0.001		
T_{delay} (s)	0.001		
V_{recon}(pu)	0.9	0.7	1
T_{recon} (s)	5	0.2	*
T_{ramp} (pu/s)	0.2 (5 second ramp to full)	**	50

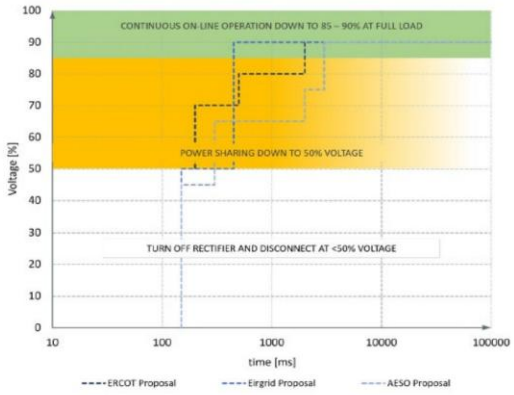
*UPS reconnection time is configurable
** UPS input power ramp-up time is configurable

Depending on UPS loading, the input active power consumption may reduce as voltage decreases as the UPS rectifier limits input current and draws the required additional energy from batteries. At full load, the rectifier current limit is typically hit around 0.85 pu input voltage.

Figure 71: Traditional slow reconnection of Eaton UPS.

Eaton 3-phase UPS – with Fault Ride Through

Parameter	Suggested generic (typical) value	Minimum (if a range is available)	Maximum (if a range is available)
V_{cease} (pu)	0.5	0.5	0.9
T_{cease} (s)	0.001		
T_{delay} (s)	0.001		
V_{recon}(pu)	0.9	0.7	1
T_{recon} (s)	0.2	0.1	*
T_{ramp} (pu/s)	20 (50 ms ramp to full)	**	50



*UPS reconnection time is configurable
** UPS input power ramp-up time is configurable

Depending on UPS loading, the input active power consumption may reduce as voltage decreases as the UPS rectifier limits input current and draws the required additional energy from batteries. At full load, the rectifier current limit is typically hit around 0.85 pu input voltage.

Figure 72: Updated ride-through-type reconnection of Eaton UPS.

The model developed in this report supports flexible configuration of tripping and reconnection logic, while coordinating the control of the rectifier, battery, and inverter throughout the process. The configuration parameters for both fast and slow reconnection are provided in the model. The fast and slow reconnection logic is illustrated in Figure 73. The reconnection delay time can be configured within the UPS VRT module, as described in Section 5.2, while the rectifier ramp-rate parameters are specified in the rectifier control settings, as discussed in Section 3.3.4.

Figure 74 further illustrates the mode transitions, voltage, and power responses associated with the VRT curve and the definition of reconnection delay time.

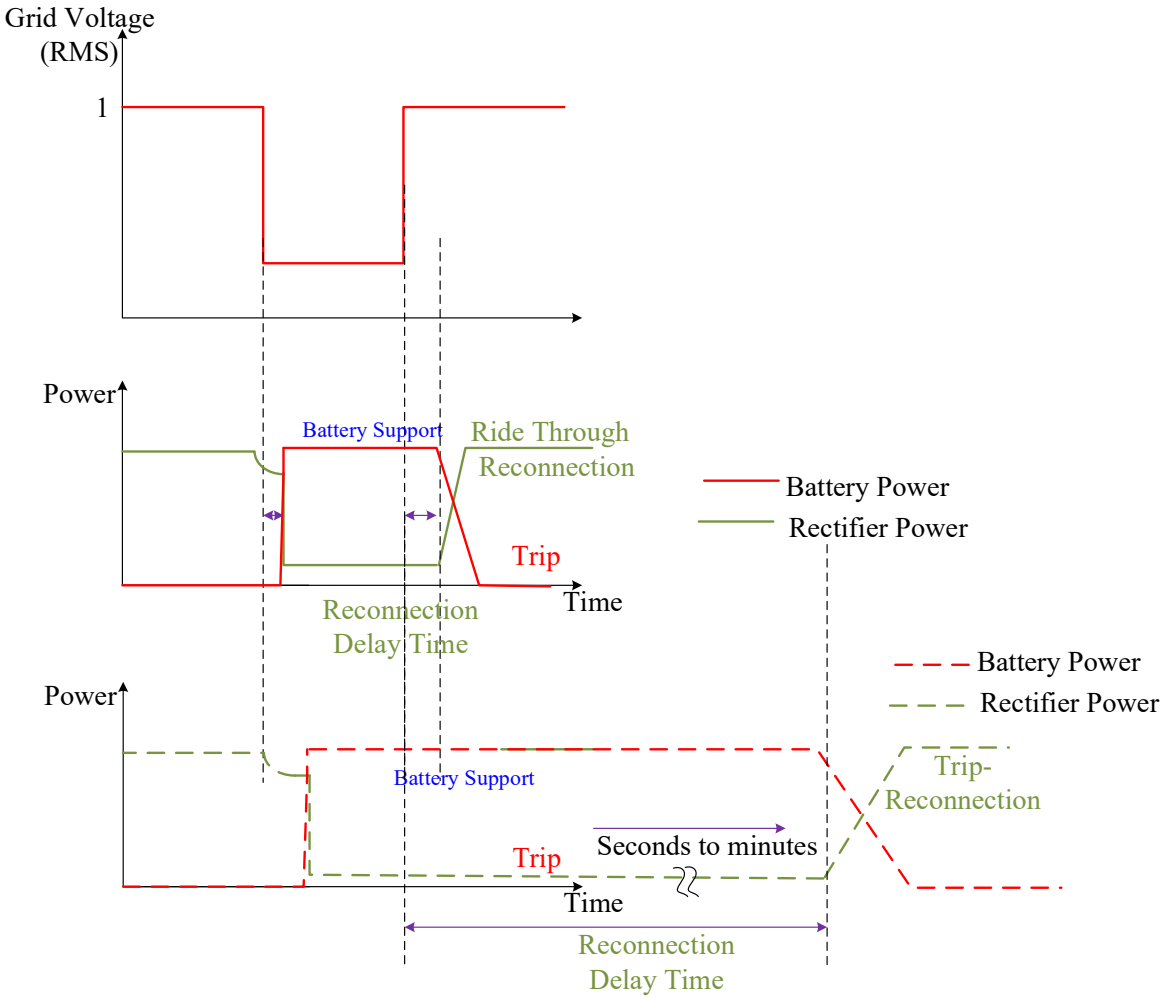


Figure 73: Ride-through and trip- type reconnection time series diagram and parameters.

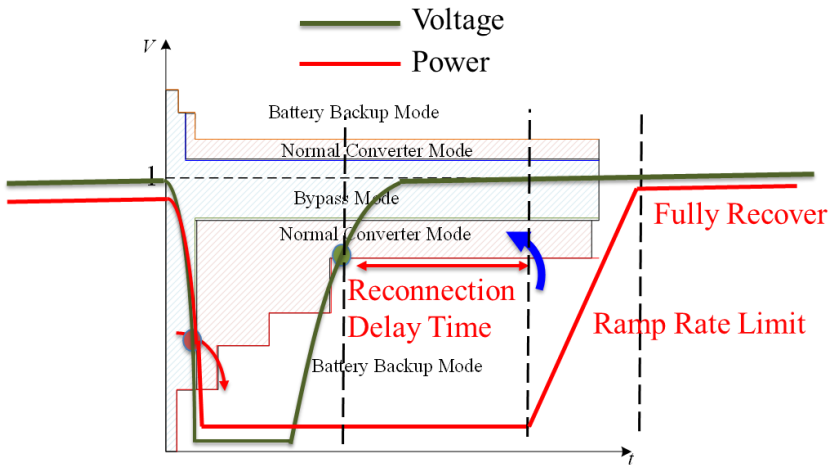


Figure 74: Mode transition logic for trip and reconnection of the rectifier.

6.3.2.2. Test Case

1) Fast reconnection

The rectifier tripping and reconnection logic is configured such that the reconnection delay after grid-voltage recovery is set to 0 s. In other words, once the grid voltage exceeds 0.6 pu, the rectifier immediately initiates reconnection. The reconnection ramp rate is set to 20 pu/s. The results are shown in Figure 75.

Before t = 4s, the system operates in normal converter mode, where the rectifier supplies the load, and the battery remains in charging mode. At t = 4s, the grid voltage suddenly drops to 0 pu and remains at this level for 0.1 s. The VRT protection issues a rectifier trip command, and the battery immediately takes over and discharges to regulate the DC-link voltage and supply the load.

At t = 4.11s, the grid voltage recovers (higher than 0.6 pu). The rectifier reconnects immediately and operates in active power control mode. Due to the ramp-rate limitation of 20 pu/s with 1MW base (13.3 pu/s with 1.5 MW base), the rectifier requires approximately 0.05 s to restore its rated power. During this ramping period, the battery continues operating and regulates the DC-link voltage. As the rectifier output increases, the battery's discharging power correspondingly decreases.

At t = 4.16 s, the rectifier fully recovers and resumes supplying the entire load, after which the battery exits discharging operation.

Under the fast reconnection setting, it can be observed from the grid power dynamics (with P_Grid shown as the black curve in the sixth subplot in Figure 75) that the grid only experiences a power loss during the period when the voltage drops to zero. Once the voltage recovers, the load is rapidly restored. For short-duration faults, this behavior is beneficial for maintaining frequency stability.

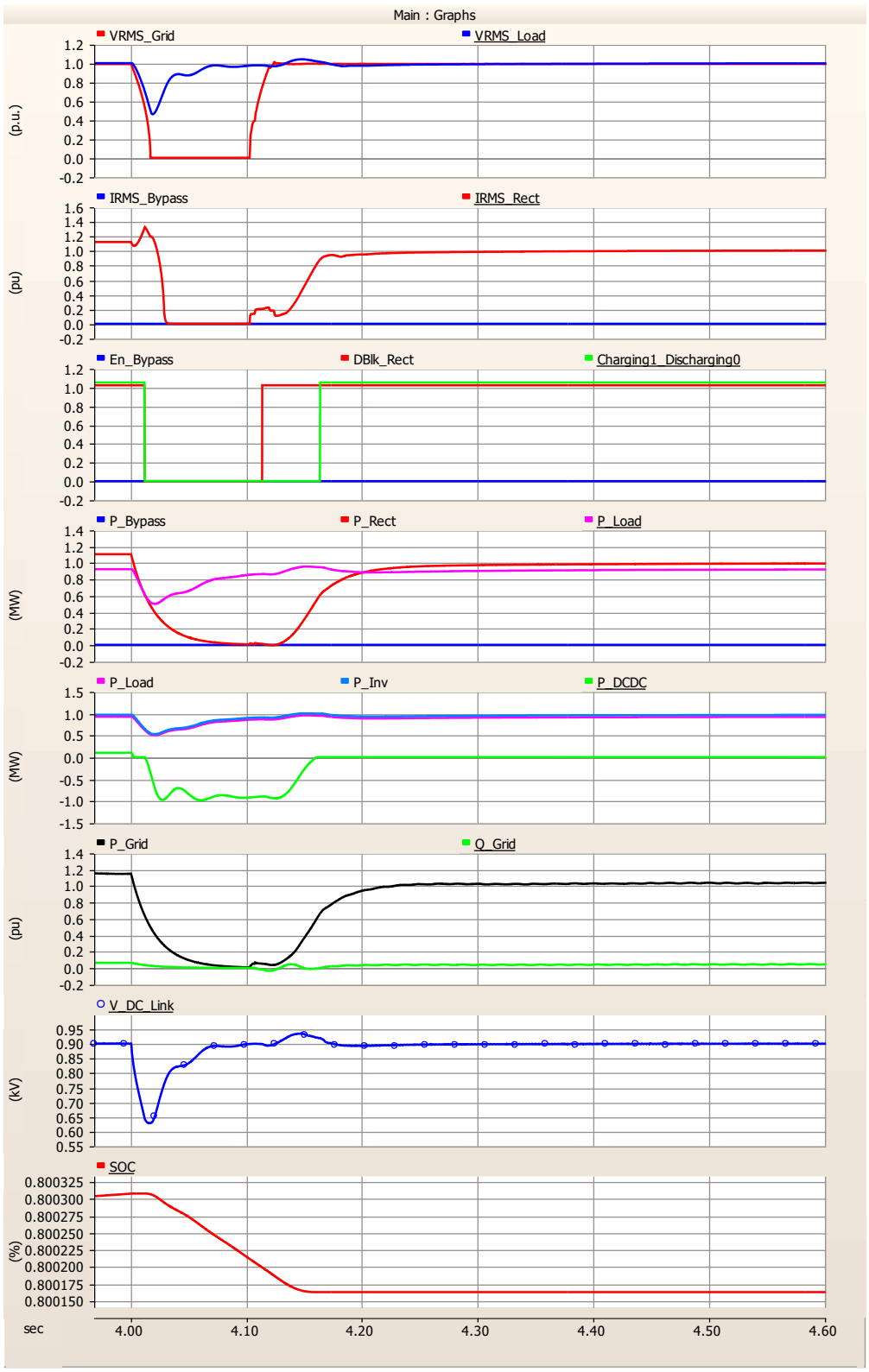


Figure 75: Fast ride-through reconnection case (reconnection delay time: 0s, rectifier reconnection ramp rate: 20 pu/s). Refer to Figure 60 for the variable name definitions.

2) Slow reconnection

In this case, the reconnection delay is set to 1 s, representing a prolonged load interruption on the grid side. This corresponds to the slow reconnection scenario discussed in this report. The simulation results are shown in Figure 76.

After the 1 s delay following the grid voltage recovery, the rectifier initiates reconnection with a ramp rate of 1 pu/s in 1MW base (0.7 pu/s in 1.5 MW base). During this period, the battery continues regulating the DC-link voltage, while the rectifier operates in active power control mode.

As the rectifier output gradually increases and eventually takes over the full load, the battery exits discharging operation. Subsequently, the rectifier transitions from active power control mode to DC-link voltage control mode to regulate the DC-link voltage under steady-state conditions.

Under the slow reconnection configuration, the grid power profile P_Grid (black curve) in Figure 76 shows a complete trip lasting approximately 1 s. This indicates a large load disconnection during this period. The load is then gradually reconnected, and full recovery is not achieved until about another 1 s later. This may lead to noticeable deviations in grid frequency.

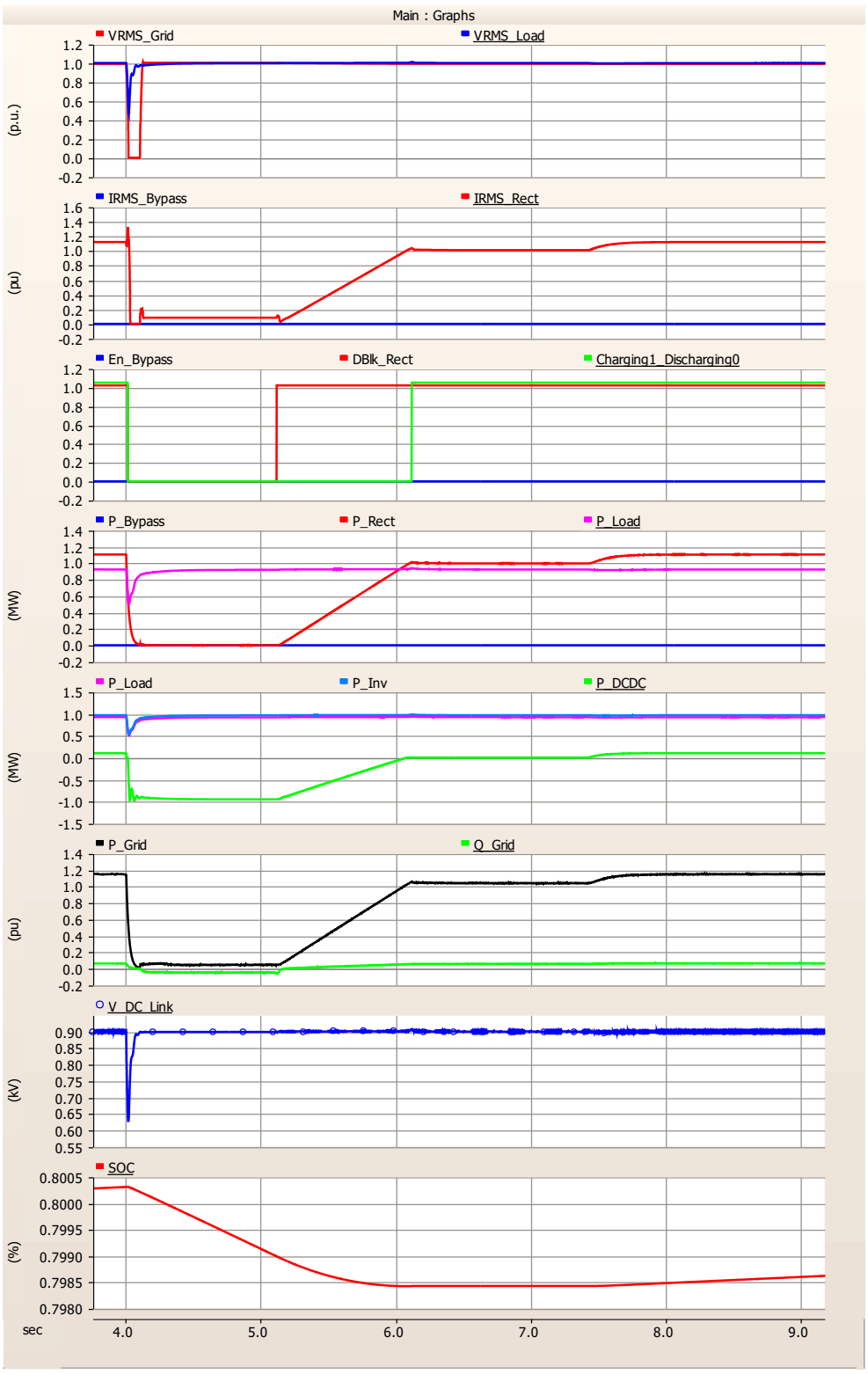


Figure 76: Slow reconnection with a reconnection delay of 1 s. Refer to Figure 60 for the variable name definitions.

6.4. Load Fluctuation (Time-Varying Computing Load)

Large-scale AI training workloads that run across tens of thousands of GPUs create distinctive power management challenges because their power demand varies significantly during training and inference. Since these jobs operate synchronously, each iteration includes a compute-intensive phase, in which every GPU processes local data, followed by a communication-intensive phase, in which all GPUs synchronize. Because the compute-intensive phase consumes substantially more power than the communication phase, these workloads produce large swings in power demand.

In the PSCAD model, the computing load is represented as a time-varying load. A load fluctuation profile can be imported through a file-based interface, enabling the direct application of time-series computing power demand in the simulation.

In this case study, a segment of GPU power consumption data from the MIT Super Cloud dataset [6] is used as the computing load profile. The data are imported into PSCAD using the Data File Reader module from “ComputingLoad.txt”, as shown in Figure 77.

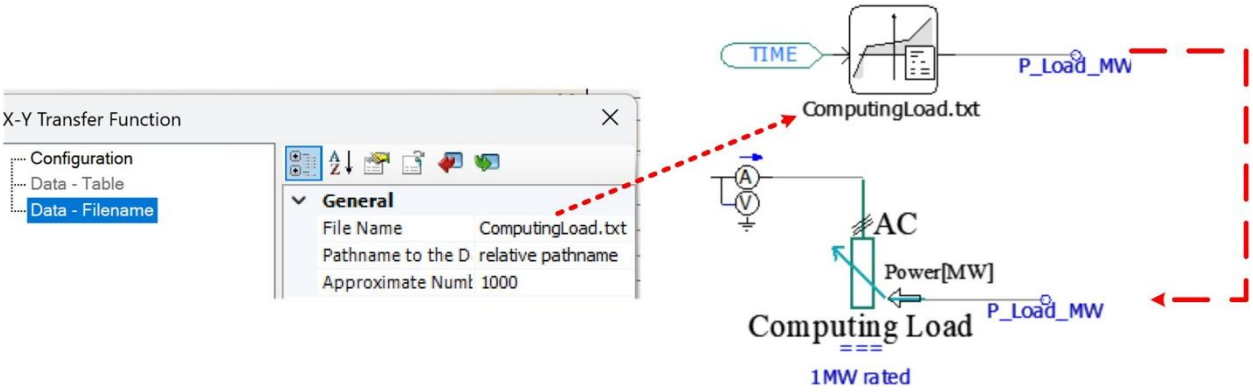


Figure 77: Computing Load Profile Input in PSCAD.

Since the original dataset has a sampling rate of 10 Hz (i.e., 0.1 s per sample), interpolation is applied during the simulation to obtain a continuous load profile.

The resulting grid-side dynamic response and UPS DC-link voltage dynamics are presented in Figure 78 to illustrate system behavior under realistic computing load fluctuations. It can be observed that load variations induce significant fluctuations in

rectifier power, which are propagated to the grid side. Meanwhile, the DC-link voltage also exhibits corresponding variations around [OBJ], the magnitude of which depends on the response speed of the rectifier DC-link voltage control loop and the UPS DC-link capacitor value.

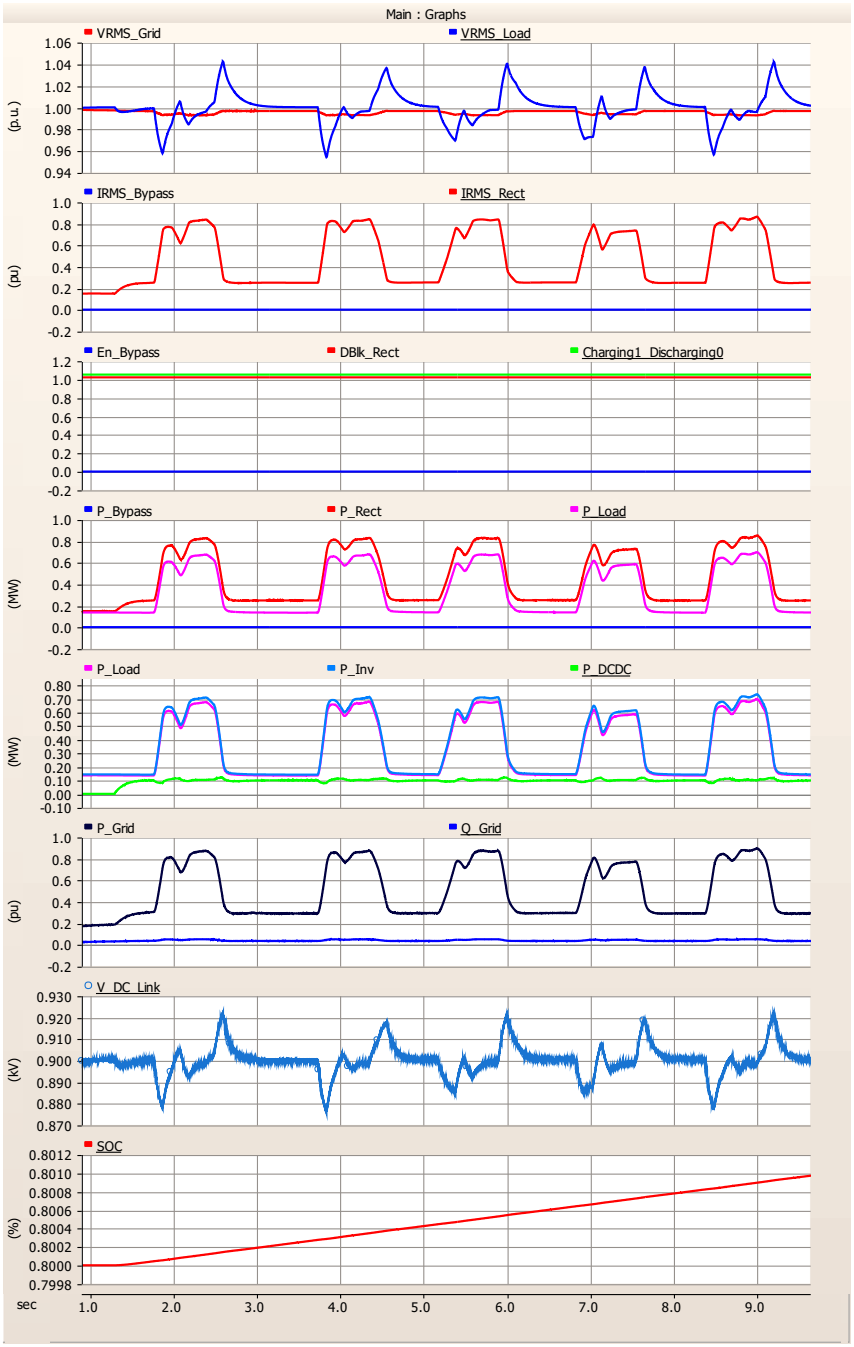


Figure 78: Dynamics during computing load fluctuation depicting large swings in power demand. Refer to Figure 60 for the variable name definitions.

It should be noted that the purpose of this case study is to demonstrate the capability of the developed model to incorporate dynamically varying computing loads. In practice, the computing load connected with the inverter represents an aggregated demand. The time-series dynamics of an individual GPU, shown in Figure 78, do not necessarily reflect the behavior of the aggregated computing load across multiple server racks. The overall load profile depends on the coordination among racks (e.g., synchronous or asynchronous operation), which determines the degree of smoothing or amplification of load fluctuations.

7. Conclusion and Future Work

This report presents a comprehensive open-source PSCAD EMT model for double-conversion UPS-based AI data centers. A model library of key component modules is developed, including the rectifier, inverter, bidirectional DC/DC converter, battery, VFD-based cooling load, and computing load, each represented by both switching models and average models. In addition, average models are compared with the switching models, demonstrating that the average models can significantly improve simulation efficiency while preserving the essential low-frequency dynamics. A centralized voltage and frequency ride-through module is also developed to represent protection logic and mode transitions, as well as tripping and reconnection behavior. The model further captures several operating scenarios, including voltage sag events, fast and slow reconnection strategies, and power fluctuations caused by time-varying computing loads. Simulation results verify the capability of the developed model to represent UPS dynamics and capture critical interactions between the data center and the power grid.

Future work will extend the developed model to incorporate additional AI data center electrical architectures, including distributed battery-based architectures, low-voltage DC distribution architectures, and solid-state-transformer-based medium-voltage architectures. It will also investigate advanced control strategies to mitigate load fluctuations and improve ride-through performance under grid disturbances.

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