Guideline for Model Quality Test in PGRR144 – DWG Procedure Manual Updates
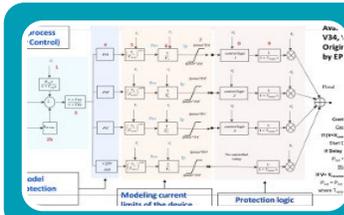
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LLWG, March 13, 2026

Background: PGRR144

- **PGRR144**
  - Dynamic Model Submission and Review Requirements for Large Loads (LLs), including Large Electronic Loads (LELs)
  - Submitted: February 2026

 Clarifies dynamic data requirements and require model quality test

 Clarifies LL dynamic model data submission milestones for review

 Clarifies process for potential material changes to the existing LELs

Model Quality Testing Framework (PG 6.2(6) in the PGRR)

- Site-specific Model Quality Test (MQT*) (All **LLs**)
  - Flat Start Test: Verifies proper model initialization and stable response under no disturbance
  - Large Voltage Disturbance (VRT) Test: modeled voltage ride-through capability at the POI under large disturbances
  - Demonstrate dynamic model meets the performance requirements
  - The MQT must be performed using PSS/E, PSCAD, and TSAT (if PSS/E UDM is used)

- Converter Model Validation Test (CMV*) (**LELs** only)
  - Hardware-type validation for the UPS converter and associated computational load
  - Demonstrate accuracy of the PSCAD model of the converter type
  - Large Voltage Disturbance (VRT) Test
  - Subsynchronous Test (frequency scan sweep)

- MQT requirement for LEL vs Non-LEL
  - For LEL facilities, MQTs are required to demonstrate that the model of the project meets the ride through criteria (e.g., proposed voltage ride through requirements in the ongoing NOGRR282)
  - For non-LEL facilities, MQTs are required, with the purpose of improving understanding of voltage ride-through capability

*Note: Guidance on MQT and CMV is available in the draft DWG Procedure Manual posted on today's LLWG website.

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Draft Updates of the DWG Procedure Manual - MQT (for LLs) and CMV (for LELs)

- **Draft DWG Procedure Manual updates for LL MQT and LEL CMV** are posted on today's LLWG website

- The MQT simulation setup is consistent with the current DWG PM Section 3.1.5.1 — Single Machine Infinite Bus with adjustable voltage for testing — except that the LL facility is connected to the infinite bus.

3.1.5.16 Large Load Model Quality Test

The purpose of this test is to determine the dynamic response of the large load to voltage deviations and help confirm the voltage ride through capability of the large electronic load per Section 2.15 of Nodal Operating Guide. The test shall be performed for the PSS/e and PSCAD models and for the TSAT model when applicable. With the load facility connected to an infinite bus whose voltage can be varied for testing, simulate the following ride-through curve. The three voltage disturbances may be tested in separate simulations if not practical to test within the same simulation.

Large Loads required to ride through per Section 2.15 of Nodal Operating Guide shall remain connected to the Transmission Grid. Additionally,

- For voltages in the normal range 0.9 to 1.1 pu and for voltages between 1.1 and 1.2 pu for up to two seconds, the Large Load shall continue consuming power from the grid at the pre-disturbance value.
- For voltages between 0.5 pu and 0.9 pu, the LEL shall continue consuming active power from the grid but may reduce consumption proportional to the lower voltage. In addition, the load shall return to 90% consumption within 2 seconds of the voltage at the POIB returning to above 0.90 per-unit. These requirements apply unless exempted according to Section 2.15 of Nodal Operating Guide.
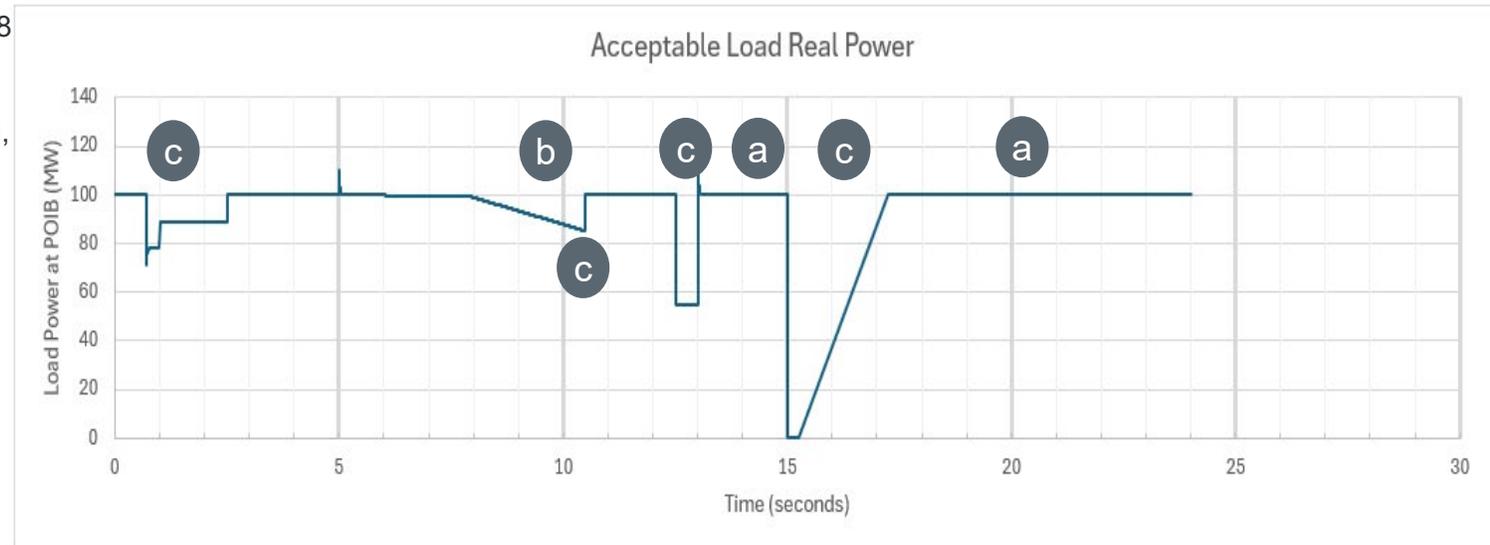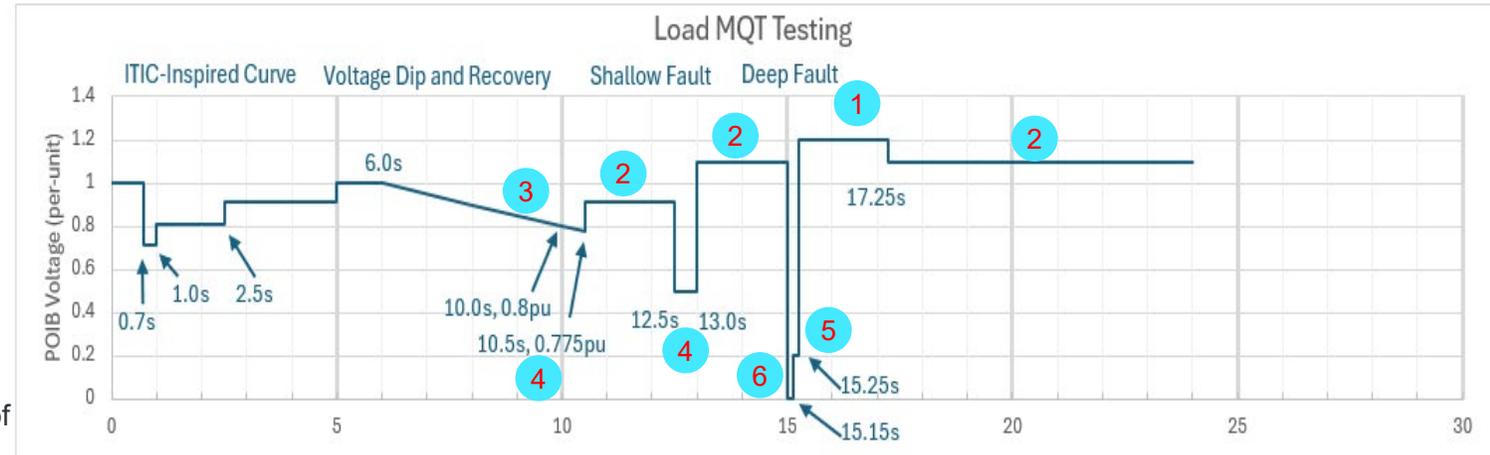
Large Load Voltage Ride-Through Test (VRT)

Reference: NOGRR282

a LELs shall continue consuming active power at the pre-disturbance level when voltage is between 1.1 and 1.2 pu for <2 sec → Section 2.15(3)(a) in **NOGRR282**

b When voltage drops to 0.8 - 0.9 pu range, the LEL may reduce proportional to voltage but should recover to 90% of the pre-disturbance power within 2 seconds of voltage recovering above 0.90 pu → Section 2.15(3)(b) in **NOGRR282**

c For voltages below 0.80 pu, the LEL may reduce its consumption but shall return to 90% of pre-disturbance consumption within 2 seconds of voltage returning to above 0.90 pu.
For LEL qualifying under the initial date range in **NOGRR282** Section 2.15(3)(c)(i) (i.e., 11/14/25-1/1/28), for voltages between 0.5 pu and 0.8 pu, the power drop should be proportional to voltage **if capable**
For LEL qualifying under the date range in **NOGRR282** Section 2.15(3)(c)(ii) (i.e., after 1/1/28), for voltages between 0.5 pu and 0.8 pu, the power drop should be proportional to voltage

Table A

Root-Mean-Square Positive Sequence Voltage (p.u. of nominal)	Minimum Ride-Through Time (seconds)	
V > 1.20	May ride-through or trip	
1.10 < V ≤ 1.20	2.0	1
0.90 ≤ V ≤ 1.10	Continuous	2
0.80 ≤ V < 0.90	2.0	3
0.50 ≤ V < 0.80	0.5	4
0.20 ≤ V < 0.50	0.25	5
V < 0.20	0.15	6

* The test curve and examples are available in the DWG PM Section 3.1.5.16

Converter Model Validation (CMV) Test for LEL – Section 3.1.6 of DWG Procedure Manual

3.1.6 Unit Model Validation / Converter Model Validation

PSCAD models must be accompanied with results from the unit model validation tests performed by the Interconnecting Entity or Resource Entity as required in paragraph (5)(d) of Planning Guide Section 6.2 and also performed by the Large Electronic Load Interconnecting Entity as required in paragraph (6)(b) of Planning Guide Section 6.2. These validations shall demonstrate the accuracy of the PSCAD models against actual inverter or converter testing and should be performed for all inverter-based devices within an IBR facility and for all computer power converters and computer UPS converter systems within a Large Electronic Load facility. inverter-based device types within the facility. The test report should clarify if the IBR inverter is capable of meeting AGS-ESR requirements and that these control settings are enabled. The tests are converter/inverter specific but need not be site-specific. The report should include a description of the test set up as well as the simulation plots of relevant quantities for each test. Guidelines on how these tests should be performed, and the expected model performance are provided in the following sub-sections.

Converter Model Validation (CMV) Test for LEL – Section 3.1.6 of DWG Procedure Manual

Hardware-in-the-Loop Converter Model Validation

PSCAD Model vs Hardware
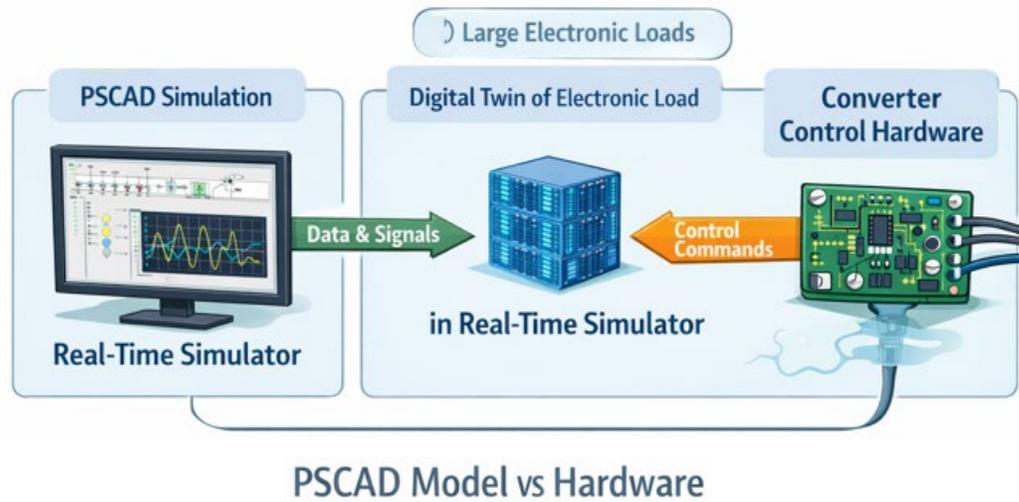
- Generally performed in OEM's laboratory. Usually performed once for a certain model or family of converters

3.1.6.3 Testing

The tests are designed to measure the inverter and model response to small and large magnitude disturbances of frequency and voltage as well as the subsynchronous response to gauge model accuracy. Many of the tests closely parallel those used in the Model Quality Guideline Section 3.1.5. Alternative testing methods may be permissible if the objective is fulfilled. Two test sections are below; the first applies to IBRs and the second applies to Large Electronic Load computer and UPS converter devices.

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The following tests should be performed on both the PSCAD model and the power electronic based converter hardware within the Large Electronic Load facility:

- o Voltage Ride Through, as specified in Section 3.1.5.16.
- o Subsynchronous Test: Perform a frequency scan sweep to measure the subsynchronous impedance as seen looking into the converter over the range 5 to 55 Hz in 1 Hz increments. This test is generally conducted by adding a small voltage perturbation of variable frequency superimposed on the fundamental (60 Hz) voltage, and measuring the complex impedance as seen looking into the inverter. The results should be provided both as a plot and as a table and should display the Resistance and Reactance plotted over 5 to 55 Hz. Values should be in ohms. The device power rating and normal operating voltage should also be reported.

Next Step

- LLWG to review and provide any comments by March 27 (Friday)

- ERCOT to share the draft DWG Procedure Manual update with the DWG in April

Questions?

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