Dynamic Modeling of Crypto-Miner Load in PSCAD

Version 7.0

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1. Introduction

In recent years, the rapid growth of large-scale crypto-mining facilities and their sensitivity to voltage disturbances have raised concerns regarding grid stability. To better understand these impacts and support transmission reliability studies, it is essential to develop accurate electromagnetic transient (EMT) models that can effectively capture their voltage-dependent dynamic behavior.

To investigate these effects, we collaborated with ERCOT to develop EMT simulation models of crypto-mining loads in PSCAD. The developed models provide the following key features and insights:

1. The crypto-miner load is modeled as a Power Factor Correction (PFC) circuit connected to a constant power load.
2. Both switching (SW) and average (Ave) models are developed. The average model omits high frequency switching to improve computational efficiency, allowing users to choose between higher accuracy or faster simulation speed depending on the study scope. Both models are benchmarked with each other, and the results are consistent.
3. The model includes DC-link low-voltage and over-current protection schemes.
4. The voltage ride-through (VRT) characteristic can be additionally defined to account for both low-voltage ride-through (LVRT) and high-voltage ride-through (HVRT) trip conditions that are not captured by DC link low-voltage and over-current protection.
5. The PSCAD models were benchmarked against laboratory test results for the device-level model. The benchmarked device model was then used to develop the facility-level model for the crypto-mining load. The facility model was subsequently benchmarked using Digital Fault Recorder (DFR) data to demonstrate its capability to accurately capture transient dynamics during voltage disturbances.

The remainder of this report is organized as follows:

Section 2 introduces the switching and average models of the crypto-miner load in PSCAD. Section 3 describes the operation scheme of the PFC circuit and its voltage and current controllers. Section 4 discusses the model validation by comparing simulated and laboratory results for LVRT. Section 5 presents impedance analysis results for both average and switching models. Finally, Section 6 provides comparison results at the device level (3.5 kW) and facility level (300 MW).

2. Modules and Components Description

In this section, we present the PSCAD implementation of the crypto-miner model. The crypto-miner is represented in the EMT domain as a PFC circuit connected to a

constant power load. Both switching and average model variants are developed in PSCAD to support simulations with different accuracy and computational requirements.

2.1. Crypto-Miner Switching Model.

2.1.1.Graphic

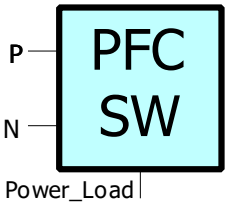


Figure 1: Graphic of Switching Model.

2.1.2.Input and Output

P: Electrical Port	N: Electrical Port	Power_Load: Control Port
AC Live Wire	AC Neutral Wire	Constant Power of Crypto-miner Load

2.1.3.Parameters

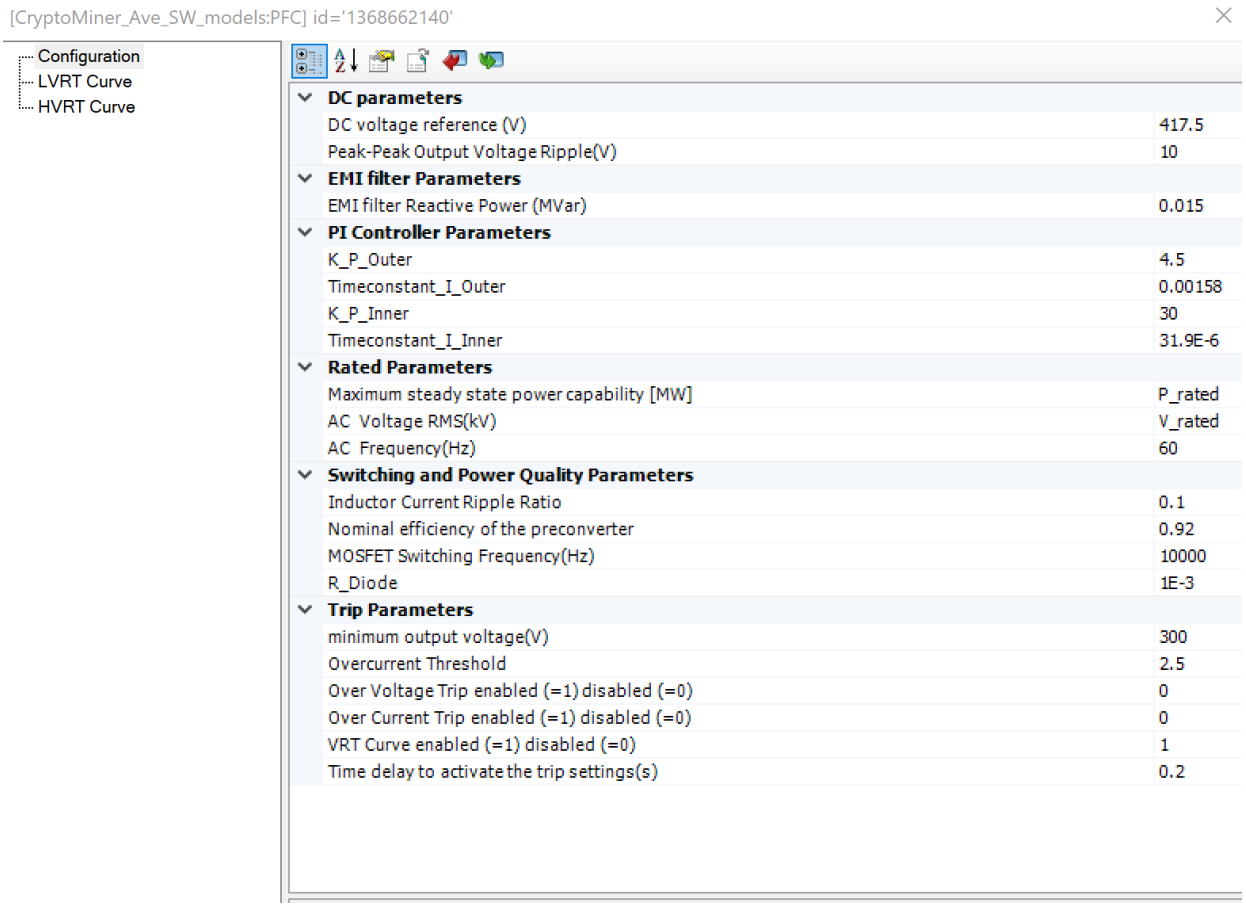
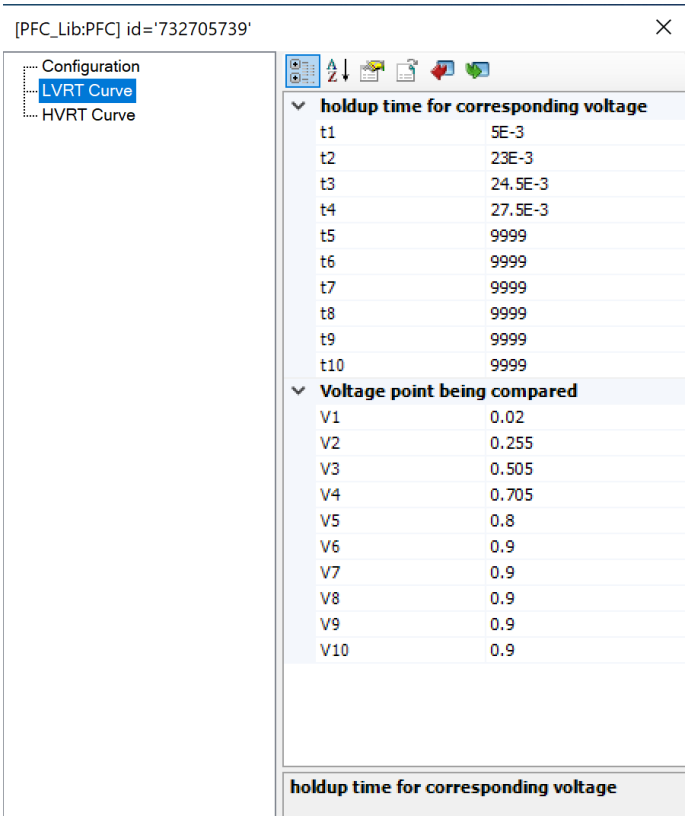


Figure 2: Parameters of switching model.

Note that R_Diode represents the equivalent resistance of the five diodes used in the switching model and is typically set to a small value, such as 0.1% of the equivalent load impedance. When VRT curve–based trip detection is enabled, both LVRT and HVRT curves must be specified, as illustrated in Figure 3. The corresponding LVRT and HVRT curves are shown in Figure 4.



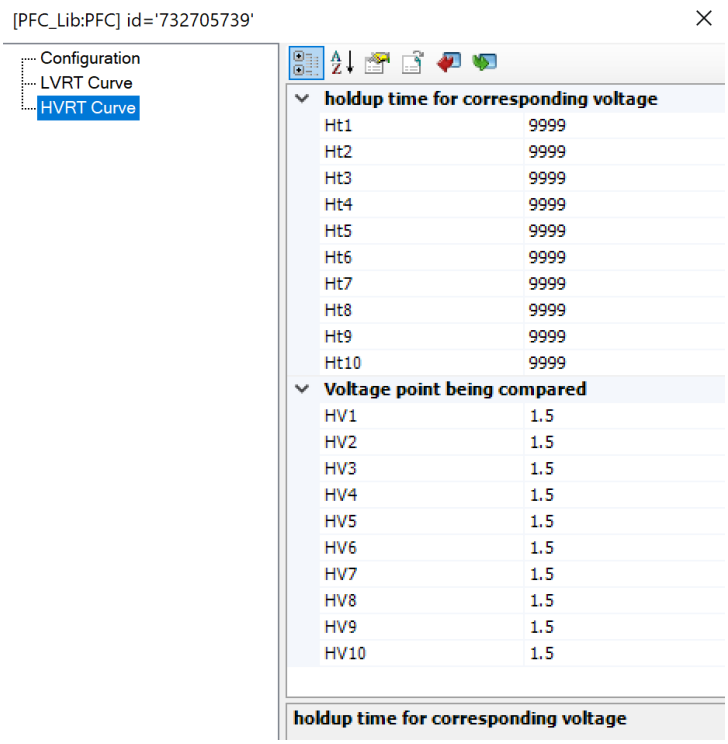


Figure 3: LVRT curve and HVRT curve.

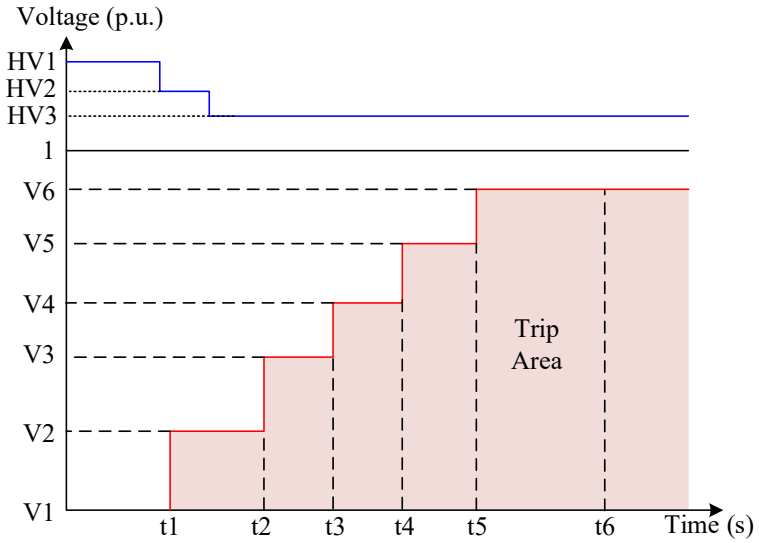
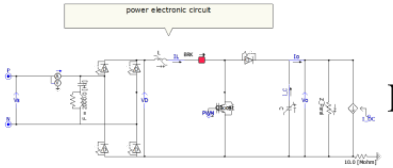


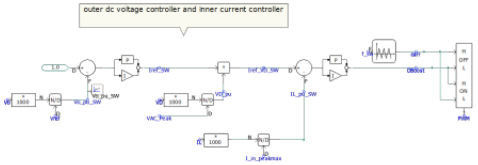
Figure 4: Illustrations of VRT curve (Here only 6 points in LVRT and 3 points of HVRT are added, in the model, can add up to 10 points for both LVRT and HVRT).

2.1.4.Model Definition

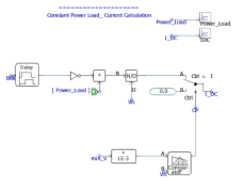
The model schematic diagram is shown in Figure 5 and includes the main power circuit, outer voltage and inner current controllers, constant power load control, protection settings, VRT mechanism, LC parameter calculations, and the section for plotting input variables and signals.



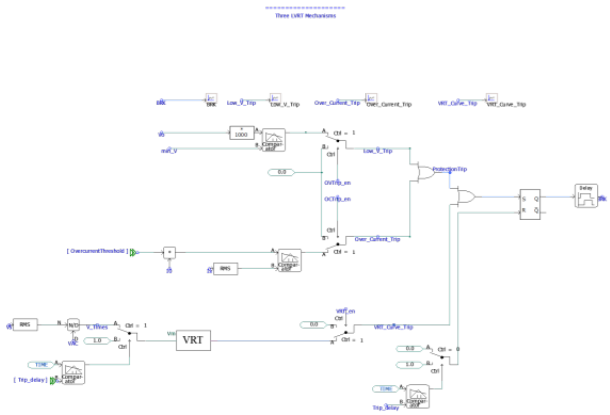
Main Power Circuit



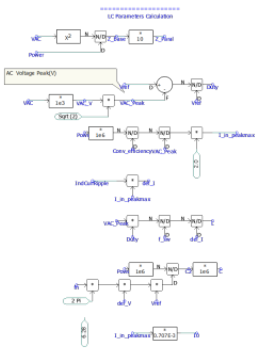
Voltage and Current PI loop



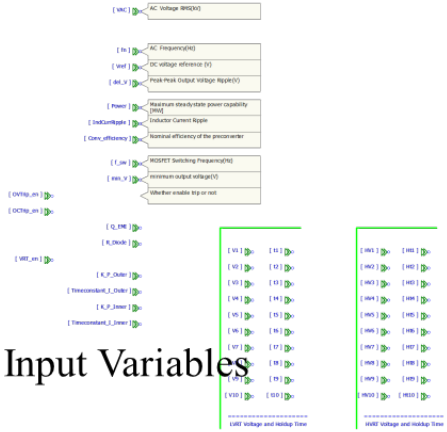
Constant Power DC Load



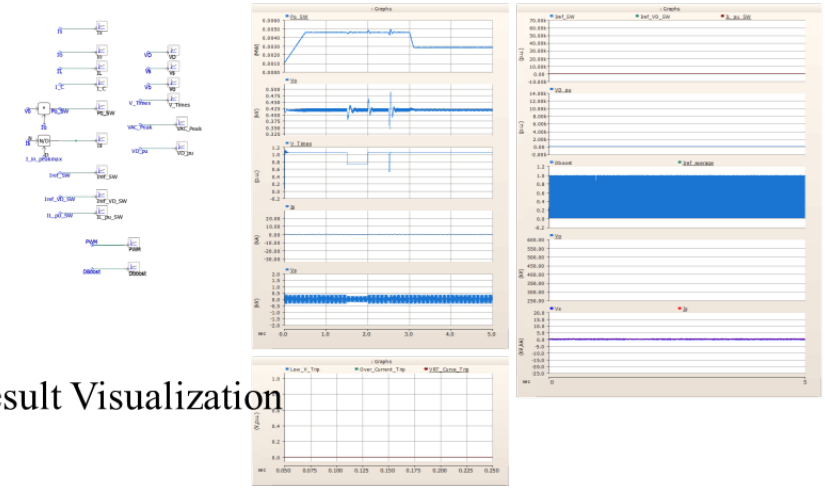
Protection scheme and VRT curve



LC Parameters Calculation



Input Variables



Result Visualization

Figure 5: Overview of switching model schematics. (The average model is almost the same).

2.1.4.1. Main power circuit

The main power circuit of the crypto-miner is the power factor correction (PFC) circuit, as shown in Figure 6. The input voltage passes through the EMI filter (capacitive filters), followed by the rectifier and the boost circuit. A virtual breaker (ideal switch) is inserted to emulate the trip mechanism.

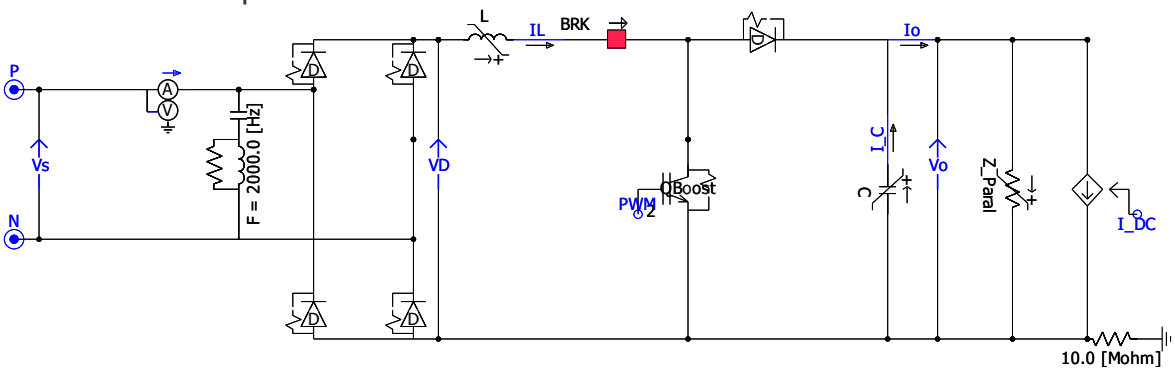


Figure 6: Definition of Switching model.

2.1.4.2. LC parameters calculation

The LC parameters are calculated automatically based on the rated power, voltage and current ripple, and DC voltage ripple, as shown in Figure 7.

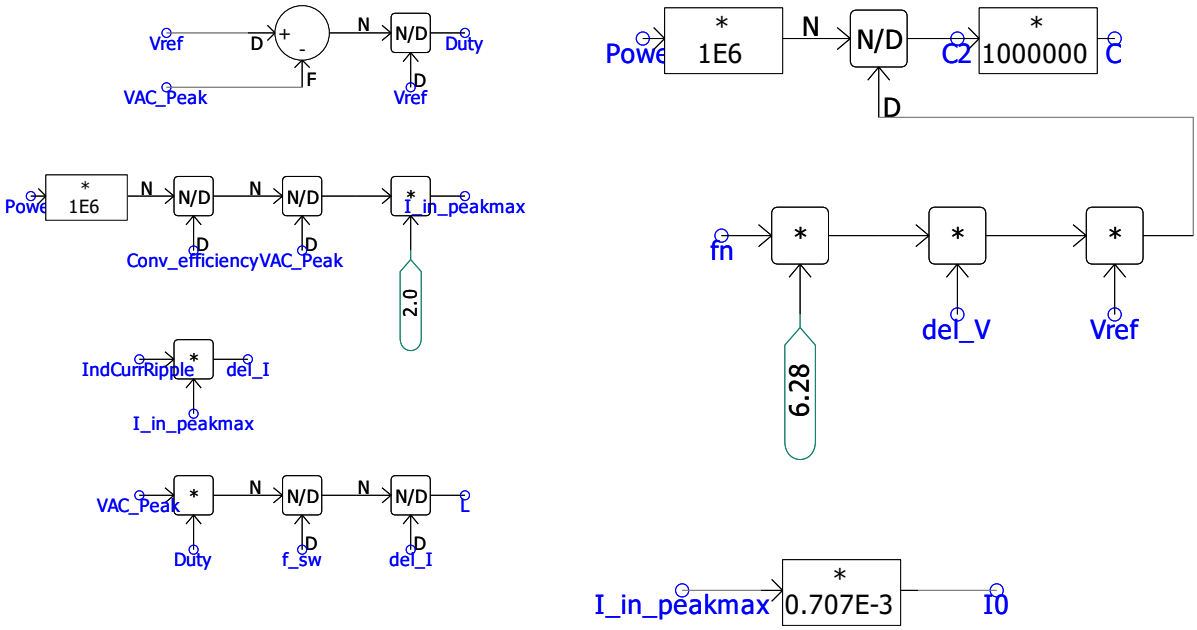


Figure 7: LC parameters calculation.

Average Duty: $D = \frac{V_o - V_{\mathrm{AC\_max}}}{V_o}$.

Where V_o means the output DC voltage. $V_{\mathrm{AC\_max}}$ means the input AC peak voltage.

The average duty represents only the mean value over a long-time scale, while the transient duty captures both the 120 Hz component and the high frequency switching oscillations above 10 kHz.

Input Current: $I_{\mathrm{AC\_max}} = \frac{2P_o}{\eta V_{\mathrm{AC\_max}}}$, where η means the efficiency and P_o means the rated output power.

Inductor Current Ripple: $\Delta I_L = \Delta I_{L,p} \times I_{\mathrm{AC\_max}}$, where $\Delta I_{L,p}$ is the inductor current ripple ratio.

Inductor value: $L = \frac{V_{\mathrm{AC\_max}} \times D}{\Delta I_L f_{\mathrm{sw}}}$, where f_{sw} means the switching frequency.

Capacitor value: $C = \frac{P_o}{V_o \times \Delta V_o \times 2\pi f_n}$, where ΔV_o is the Peak-Peak Output Voltage Ripple a user-defined parameter. f_n is the power grid frequency, which is 60 Hz.

2.1.4.3. Voltage loop and current loop PI Controller

The PI controllers as shown in Figure 8 are designed based on per-unit values. The parameters of the outer-loop and inner-loop PIs can be adjusted in the model's configuration settings. The output of current loop is the duty of boost switching IGBT. Finally, the duty is used to generate the PWM wave based on the carrier frequency.

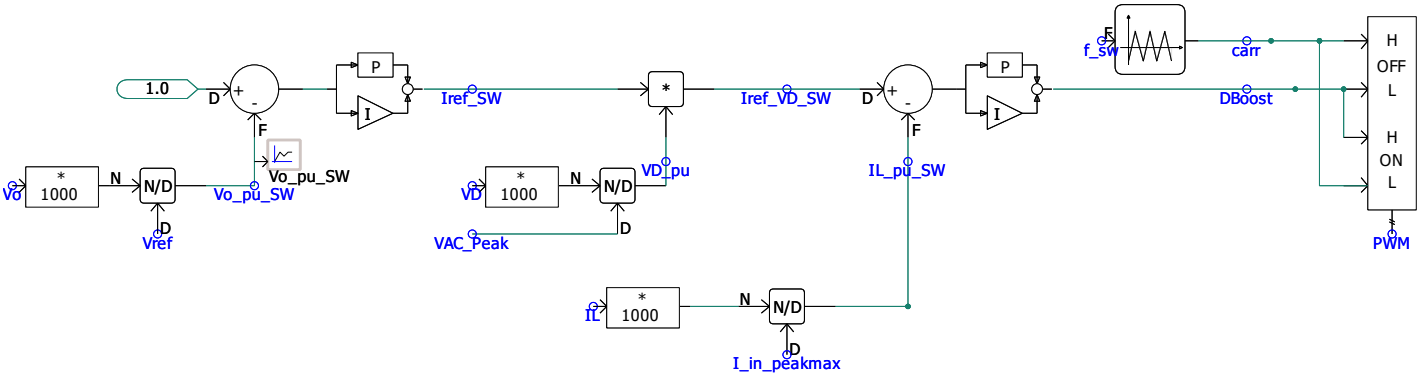


Figure 8: Controller of PFC circuit which includes outer voltage loop and inner current loop, and the PWM generator.

2.1.4.4. Constant Power Load

The constant power load is designed to model the crypto-miner load. During transient dynamics, the crypto-miner load can be seen as a constant power load. The constant power load is achieved by a controlled current source as shown in Figure 9. The current I_DC is calculated based on:

$$I_{\mathrm{DC}} = \frac{P \times BRK}{\min\{V_{\mathrm{DC}}, 10^{-3}\}}$$

where BRK is the trip signal. After a trip, the constant power load is turned off and set to zero.

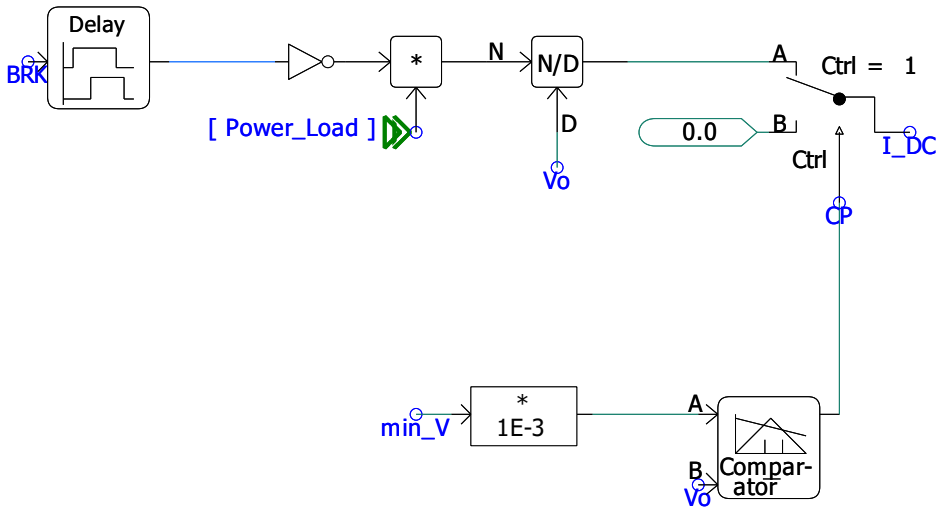


Figure 9: Constant Power Load model which is used to model the DC computing load of crypto-miner.

2.1.4.5. Voltage Ride Through Trip Mechanism

There are three types of VRT trip mechanisms, as shown in Figure 10. The trip signal passes through an SR flip-flop and will not reset unless the trip detection is manually cleared.

1) Low DC voltage trip
   The DC voltage is monitored, and if it falls below the minimum value set in the miner parameters, the trip signal is triggered.

2) Over AC current trip

   The AC current RMS value is measured and compared to a threshold defined as a multiple of the normal value. If the AC current exceeds this threshold, the trip signal is triggered.

3) VRT Curve Trip Detection (LVRT Curve and HVRT Curve)

   The AC voltage Root Mean Square (RMS) is measured and compared to the predefined LVRT or HVRT curves. If the voltage drops below the specified value for longer than the hold-up time, the corresponding trip signal is activated.

The three trip signals are combined using a logical “Or” operation.

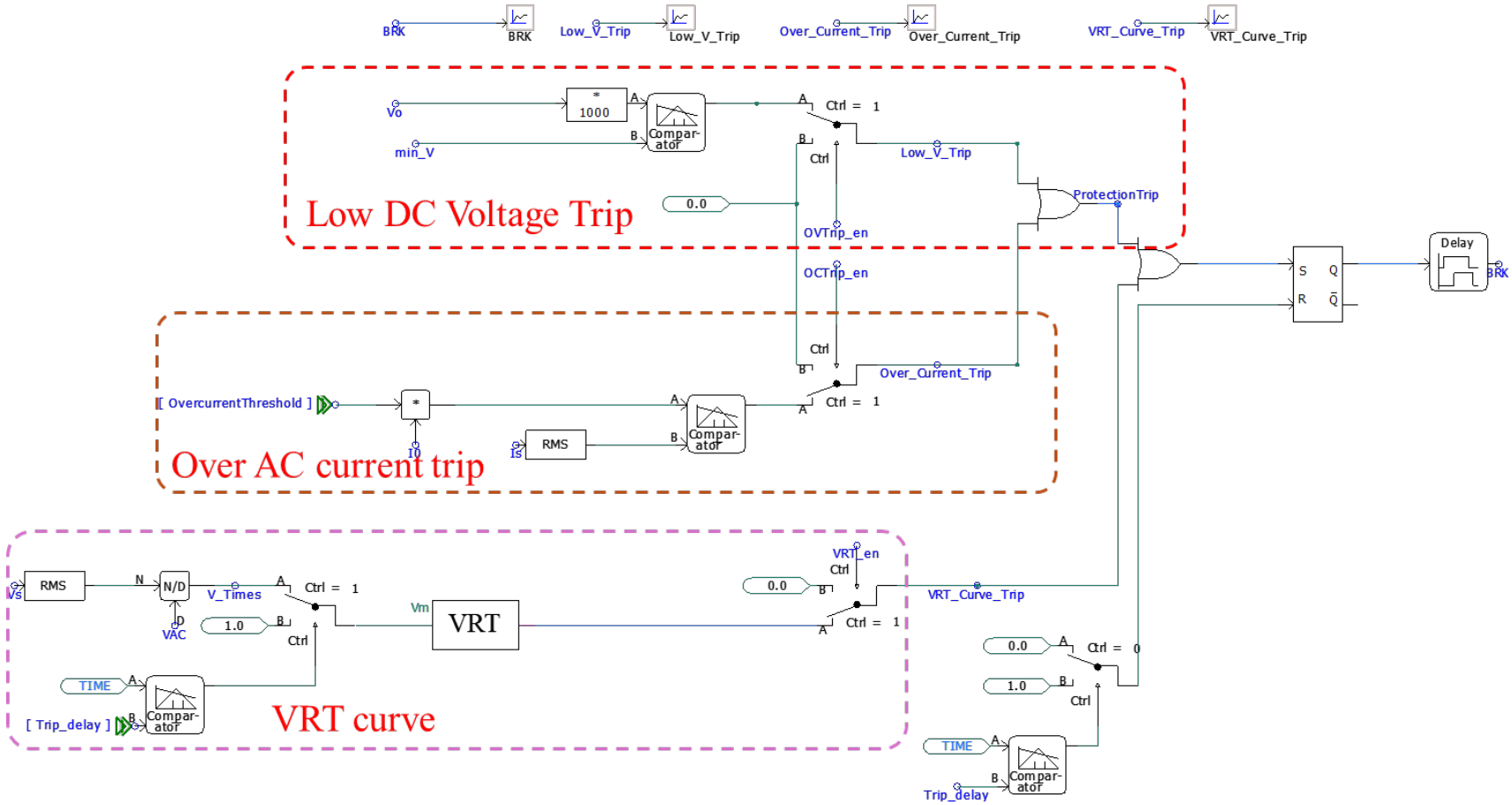


Figure 10: Protection settings and the VRT curve mechanisms.

2.2. Crypto-Miner Average Model

2.2.1.Graphic

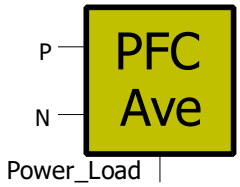


Figure 11: Graphic of PFC Average Model.

2.2.2. Input and Output

P: Electrical Port	N: Electrical Port	Power_Load: Control Port
AC Live Wire	AC Neutral Wire	Constant Power of Miner Load

2.2.3.Parameters

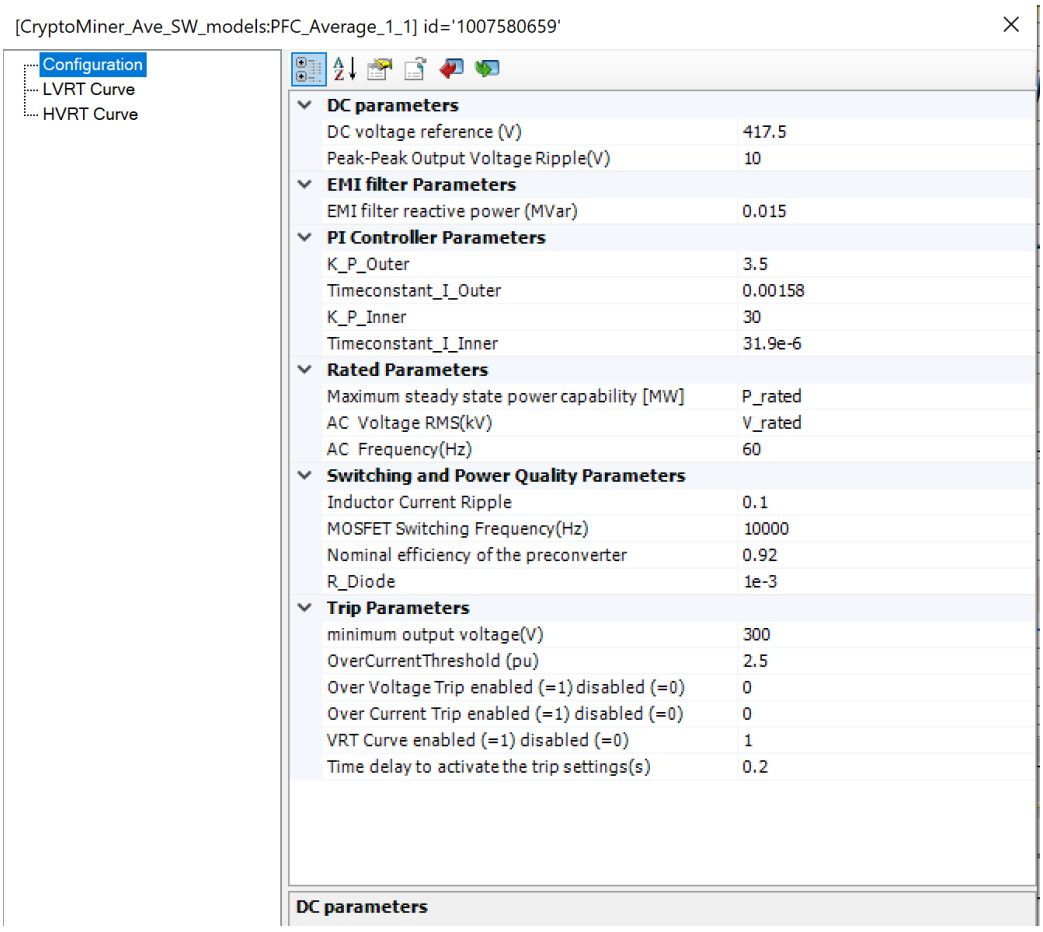


Figure 12: Parameters for the average model.

The parameters of the average model are largely the same as those of the switching model. In the average model, the switching frequency is used to calculate the inductor value and should be kept consistent with that of the switching model.

2.2.4.Model Definition

The electric circuit of the PFC average model is shown in Figure 13. A voltage source and a current source are used to represent the rectifier: the voltage is controlled based on the absolute value of the AC voltage, while the current is controlled according to the inductor current, with its direction determined by the AC voltage. For the switching IGBT, a controlled voltage source and controlled current source replace the actual switch. The voltage connected to the inductor is controlled as $D_{\text{off}}V_o$ and the current source is controlled as $D_{\text{off}}I_L$. For the details of average model, see [1] for more information.

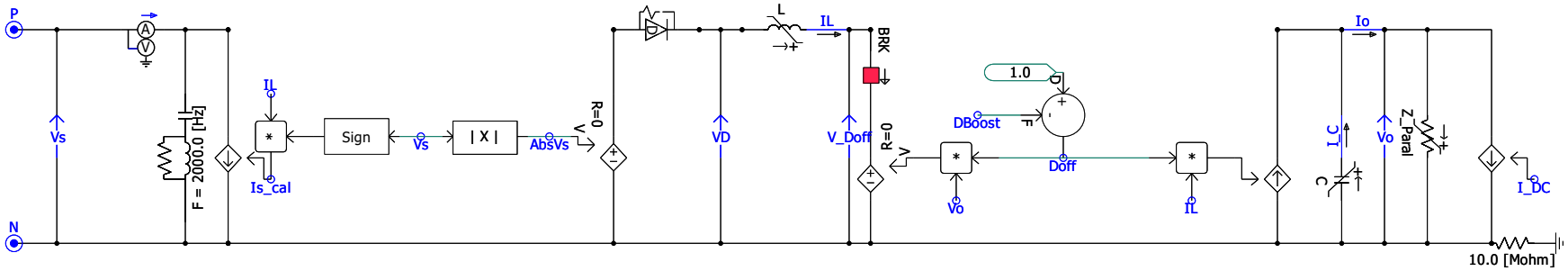


Figure 13: Model definition of average model.

The diagram of the average model is shown in Figure 14.

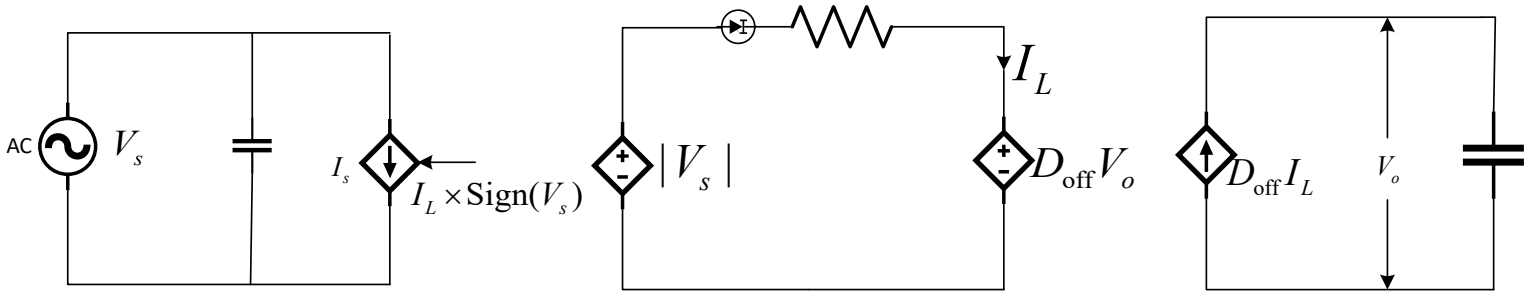


Figure 14: Diagram of average model.

where $D_{\mathrm{off}} = 1 - D_{\mathrm{on}}$, and D_{on} is the output duty of PI controller which is the same as the switching model. The other part is fully same as the switching model.

2.3. Voltage Ride-Through Curve

To match a real miner's VRT curves, a convenient approach is to use the VRT curve trip mechanism. The VRT curve-based trip detection mechanism is user-define and can be configured to match any desired VRT profile, which reflects the behavior of actual miners. In practice, VRT curves are also employed in real miners to comply with LVRT and HVRT standards, such as ITIC or IEEE 2800-2022.

As shown in Figure 15, the AC voltage is measured and compared with a preset threshold. If the voltage falls below this threshold, a timer starts, and if the voltage remains below the threshold after the delay time, the trip signal is triggered. The parameters of the VRT curve are shown in Figure 16. In this model, 10 points are defined for both LVRT and HVRT; if additional points are required, the inner model must be modified.

Figure 15: VRT Curve-based Trip detection module.

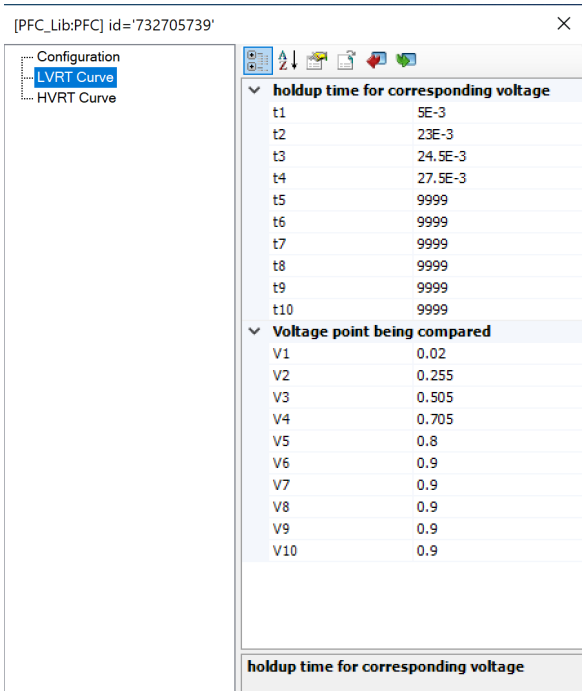


Figure 16: VRT Curve parameters.

The VRT curve trip mechanism is shown in Figure 17. The input AC voltage V_{m} is compared to a set value V_i . If V_{m} is below V_i , a delay of t_i is applied. If the voltage remains below the threshold after the delay, the trip signal is triggered. Additional comparison points can be added by duplicating the comparison components inside the module.

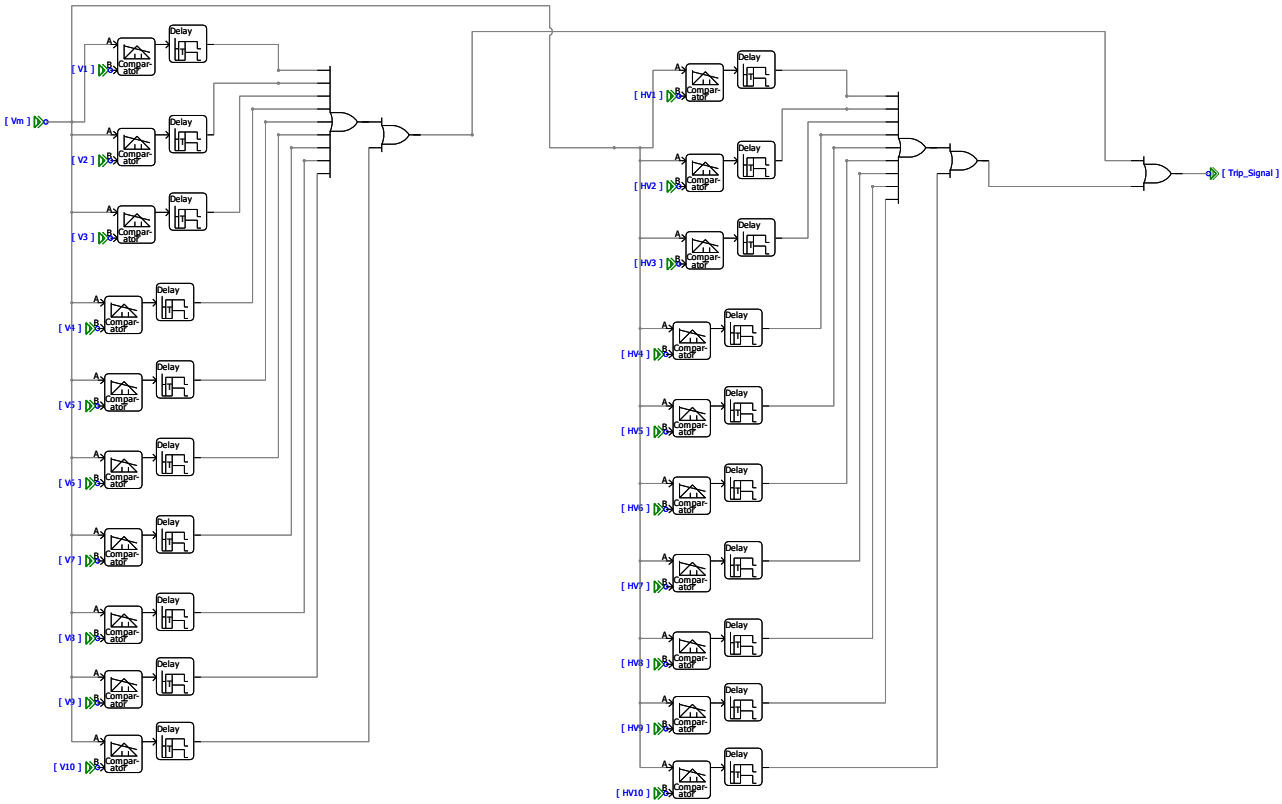


Figure 17: LVRT and HVRT Curve Implementation mechanism.

3. Power Factor Correction Circuit

In this section, we provide a description of the PFC circuit. First, the main electrical circuit and current paths of the PFC are presented. Next, the dual-loop PI controller is introduced. Finally, the sensitivity of the PI parameters and the trade-offs between voltage ride-through, overshoot, and stability are discussed.

3.1. Main Electrical Circuit

Figure 6 shows the crypto-miner load electrical circuit, which includes the following components:

1) **Diode bridge** rectifies the source voltage (V_s) into a rippled DC voltage (V_D)
2) **Boot converter** generates a smooth output voltage (V_o) across the capacitor
3) **Load** modeled as a current source and controlled to operate as a constant power load.

For the PFC applied in the miner, the source voltage Vs is **240V AC (RMS),** and the DC voltage Vo is around 400V, which feeds the miner's internal voltage regulators. The key principle of PFC is to control the source current to be in phase with the source voltage, achieving a power factor close to 1.

Unlike a full-bridge AC/DC inverter, the rectifier uses only uncontrolled diodes. To shape the current waveform, an IGBT in the boost circuit is employed. As shown in Figure 19, when the IGBT is turned on, the inductor is charged by the source (red line #1) while the capacitor supplies power to the load. When the IGBT is turned off, both the source and the inductor provide current to charge the capacitor and supply power to the load.

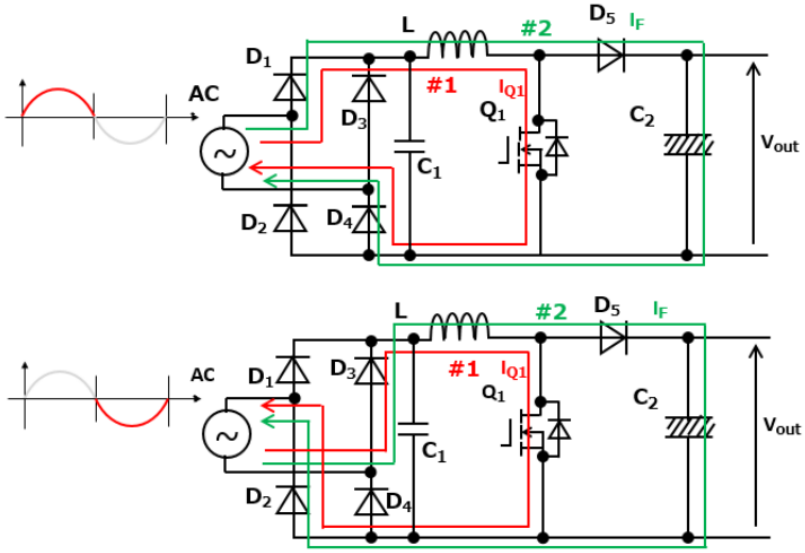


Figure 18: Current paths.

To maintain the DC voltage at a constant value, the IGBT's on-time and off-time must be controlled. Considering the average duty, *D* represents the proportion of time the IGBT is on, while (1-*D*) denotes the average turning off Duty. represents the average off-time. When the IGBT is on, the voltage on the right side of the inductor is 0; when the IGBT is off, the voltage on the right side of the inductor is *Vo*. The average voltage on the right side of the inductor is therefore $(1-\bar{D})V_o$. During steady state, the average voltage across the inductor L must be 0, leading to the following relationship:

$$(1-\bar{D})\bar{V}_o = \text{Average}(|V_{AC}|),$$

where $\bar{D}$ is the average duty, and $\text{Average}(|V_{AC}|)$ is the average rectified voltage.

3.2. Dual-Loop Control for DC Voltage Regulation and Phase Tracking

To adaptively control the output DC voltage, a voltage loop is employed, as shown in Figure 20. The input to the loop is the difference between the reference DC voltage V_{ref} (set to 1.0 in per unit value), and the measured output DC voltage V_o. V_{ref} is is a configurable parameter, typically set to 400 V. $\frac{V_o}{V_{ref}}$ is the measured DC voltage in per unit value. The output of the voltage loop is the average reference current I_{ref_SW}. When the output DC voltage is below the reference 400 V, the inductor is charged with a larger current. The transfer function of the voltage loop is given in (3.1).

$$I_{ref\_SW} = (K_P + \frac{K_I}{s})(1-\frac{V_o}{V_{ref}}) \quad (3.1)$$

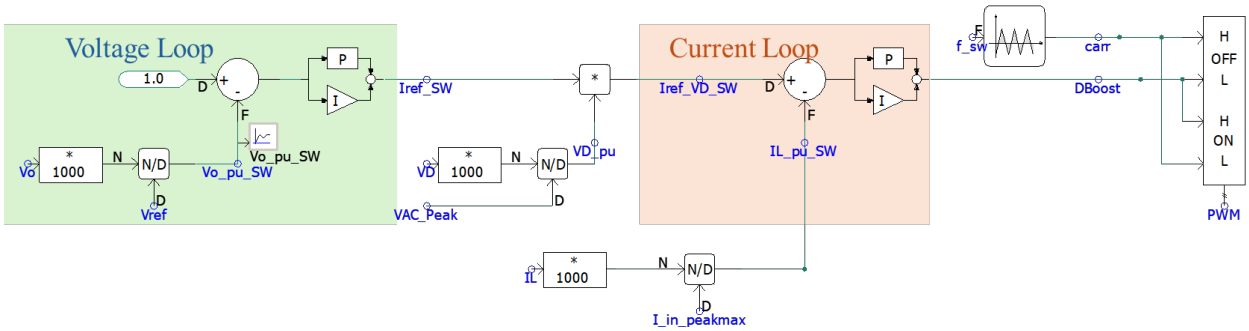


Figure 19: Dual-loop PI control for PFC circuit.

After obtaining the average reference inductor current, the transient current must be controlled to follow a rectified sine wave in phase with the rectified AC voltage V_D. To achieve this, the rectified voltage is multiplied by the average reference current I_{ref_SW} to generate the reference transient current $I_{ref\_VD\_SW}$. The rectified voltage V_D is converted to per-unit value dividing by the basic AC peak voltage, which is set as the nominal AC voltage $240\text{V} \times \sqrt{2}$. In this way, the phase information of the input voltage is extracted from V_{D_pu} as shown in Figure 21. Here, V_{D_pu} is a rectified sine wave with magnitude 1, providing the voltage phase information. This signal is then used to control the instantaneous inductor current to be in phase with the voltage, effectively serving the same role as a PLL.

The reference current is achieved by controlling the IGBT's on and off duty. To this end, a current loop is employed to regulate the IGBT switching. The reference transient current is compared with the measured inductor current I_L. The measured current I_L is converted to per-unit value I_{L_pu} by dividing by the peak value, which is calculated based on the rated current; and I_{L_pu} thus ranges between 0 and 1. For further details on the PFC circuit, refer to [1].

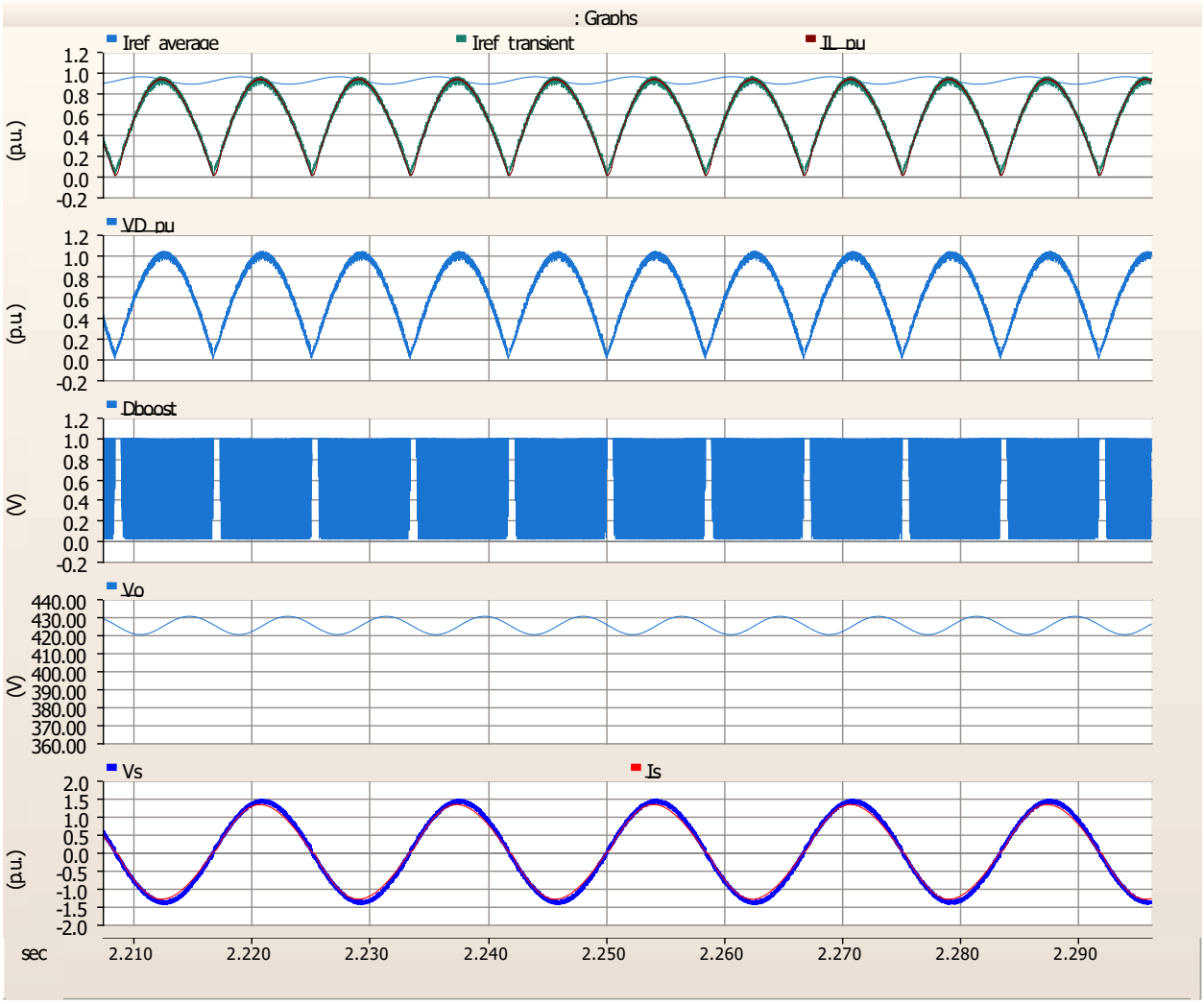


Figure 20: Inner signal of Dual-loop and the output DC voltage and input AC voltage and current in steady state.

In the average model of the PFC as shown in Figure 22, the switching IGBT is replaced by a controlled voltage source in series with the inductor and a controlled current source in parallel with the capacitor. The voltage source is controlled by $(1-D)V_o$ and the current source is controlled by $(1-D)I_L$, where D is the duty output from the dual-loop controller. For more details on the average model, refer to [1].

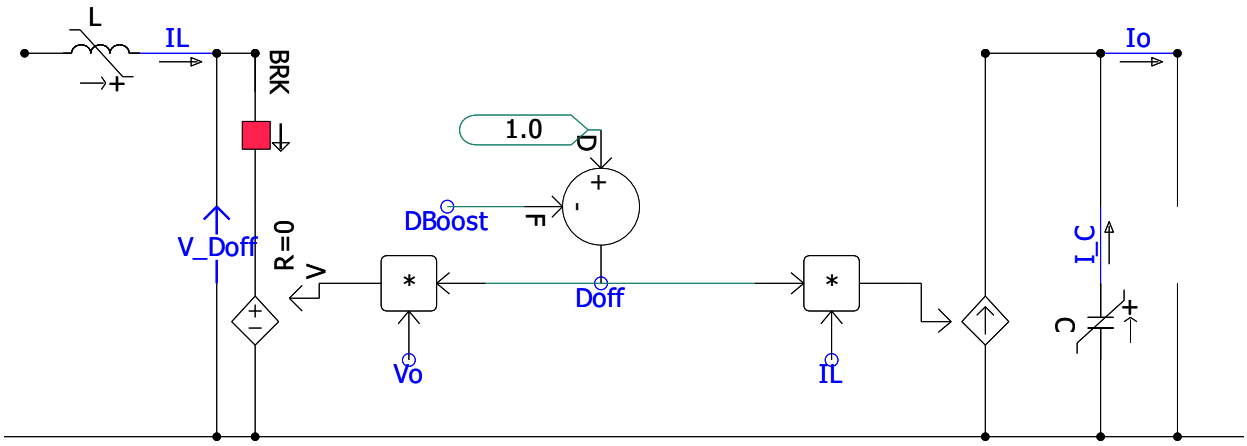


Figure 21: Average model of PFC.

3.3. PI Controller Tuning and Voltage Ride-Through

3.3.1.Role of PI Controllers in VRT

When a **voltage sag** occurs on the AC side:

- The outer voltage PI detects that the DC bus has dropped below 400 V.
- It commands the inner current loop to increase the current intake.
- The inner PI drives the boost converter switch, shaping the transient current to follow the phase of the AC voltage while increasing its magnitude according to the output of the outer voltage loop.

For a constant power load like the miner, the control loops must be carefully tuned to manage this inherently negative-impedance behavior; otherwise, the system may oscillate or trip.

3.3.2.Effects of Proportional and Integral Gains of Outer Loop

1) Voltage Dip Response Time
   - **Higher** K_P → faster correction of DC bus dips.
   - **Higher** K_I → stronger integral action to eliminate steady-state errors, but excessive values can cause overshoots.
   - **Excessively High** $\frac{K_P}{K_I}$ → potential oscillations or overcurrent surges as the system attempts to restore voltage too aggressively.
2) System Oscillations and Damping
   - Fast, high-gain loops are prone to underdamped behavior, causing ringing in the DC voltage or input current.
   - Lower gains or carefully placed poles/zeros → improved damping and more stable ride-through, though recovery is slower.
3) Power Draw Fluctuations

- During a sag, an aggressive PI controller can cause the miner to draw very high current, potentially worsening the sag for other loads or tripping its own protection.
- A conservative PI may allow the DC bus voltage to sag more (reducing power draw) to preserve stability, but gains that are too low risk under-voltage.

4) Recovery Performance
   - **High gains** → rapid restoration of bus voltage after the sag but may cause overshoot (spike in DC voltage/current).
   - **Lower gains** → smoother, but slower, return to nominal voltage.

3.3.3. Trade-Offs in PI Tuning for Large Flexible Loads

A critical trade-off exists between fast recovery (beneficial for miner uptime) and system stability (avoiding current or voltage overshoot). Tuning typically involves:

- **Bandwidth Separation**: A high-bandwidth inner current loop (~1–5 kHz) combined with a slower outer voltage loop (~5–20 Hz).
- **Moderate Phase Margin**: The voltage loop is often tuned with a generous margin (e.g., 60–80°) to handle the negative impedance effect of a constant power load.
- **Avoiding Saturation**: Clamping or limiting the PI output prevents integrator windup and control saturation during deep sags.

The voltage ride-through capability of a large, flexible load like the miner strongly depends on PI controller tuning in its PFC stage. Properly selected proportional and integral gains enable the miner to:

- Respond swiftly to AC voltage dips,
- Maintain the DC bus above its undervoltage threshold,
- Avoid damaging current surges or oscillations upon recovery.

4. Model Benchmarking

We benchmarked the PSCAD model by comparing its low-voltage ride-through (LVRT) response with laboratory test results from a real miner. The model was matched with one of the actual hardware crypto miner with a maximum power of 3.5 kW. The AC voltage is 240 V (RMS), the DC voltage is 425 V, and additional specifications are provided in Figure 23. The test device is shown in Figure 24.

Crypto Algorithm	SHA-256
Optimal Power Efficiency (Joules/TH)	16[1]
Hashing Performance (TH/s at Joules/TH)	0-260 / xx Joules/TH at xxx TH/s[1]
Operating Temperature Range	-4 to 122°F (-20 to 50°C[2])
Power Supply	5000 Watts[3], 2 x C20 Input
Power Cables Included	2 x C19 to C20
Cooling Mechanism	Air-cooled
Power Supply AC Input Voltage, Nominal, Min/Max	200-240V, 180 - 264V
Power Supply AC Input Frequency	48-62 Hz
Power Supply AC Input Current	0-17.6 Amp per input

Figure 22: Datasheet of the crypto miner

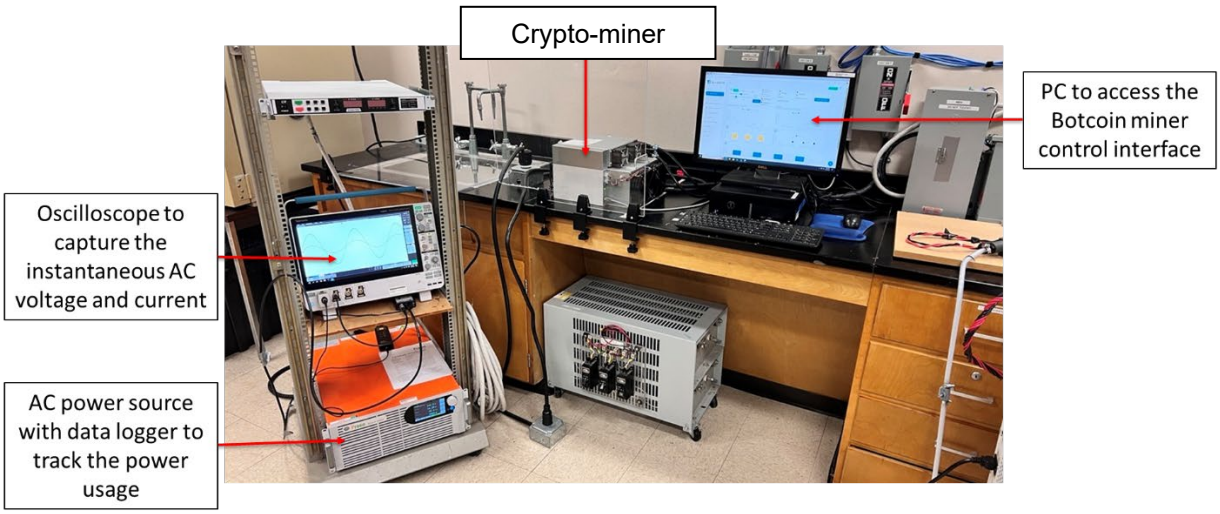


Figure 23: Real lab Test of Miner.

To verify the developed PSCAD model, two voltage sag scenarios are simulated to demonstrate that the transient dynamics closely match the real lab test results. The method for generating the faults is illustrated in Figure 25.

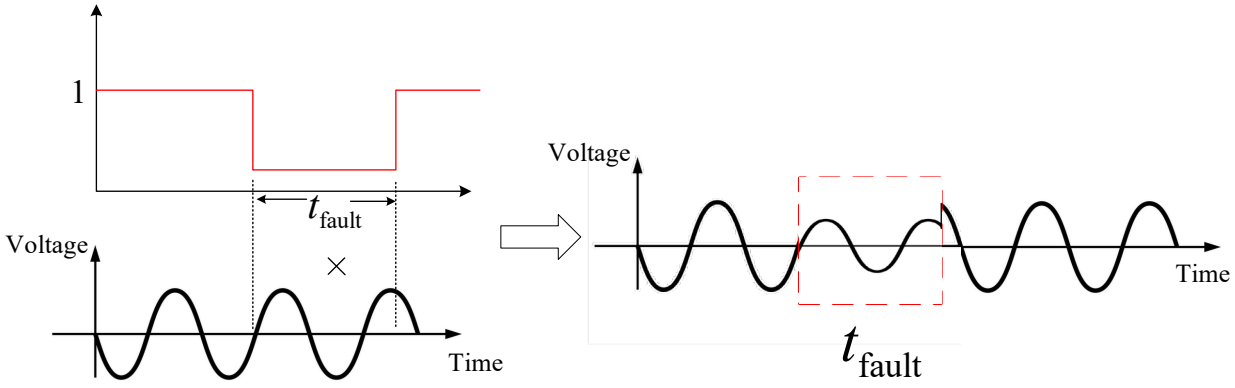


Figure 24 : Fault setting method.

In PSCAD, the test case is constructed as shown in Figure 26. with the rated power set to 3.5 kW. Additional parameters are provided in Figure 27.

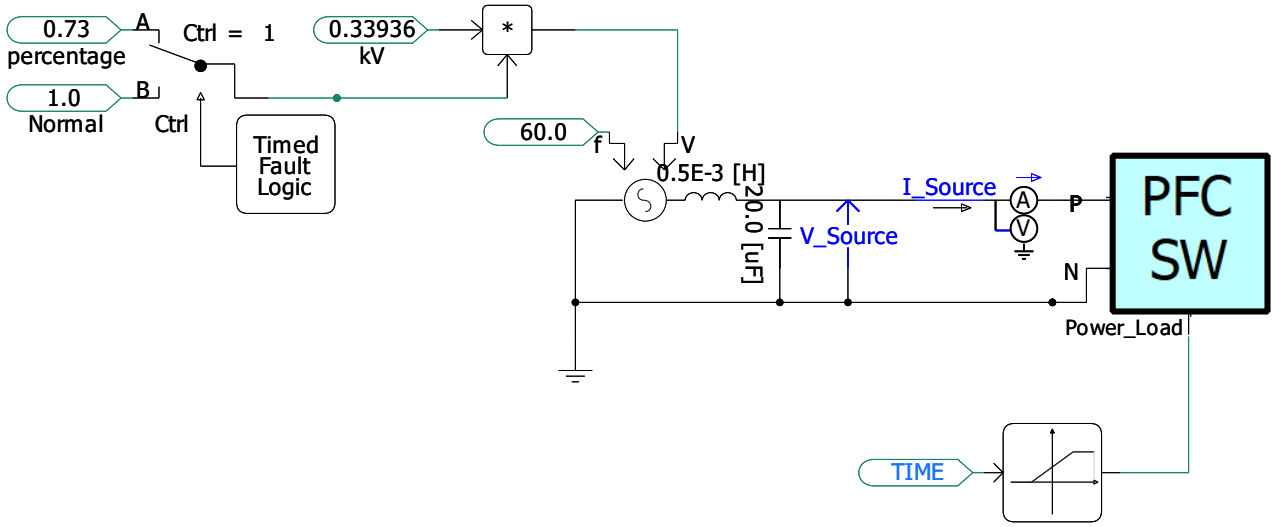


Figure 25: PSCAD case for model validation.

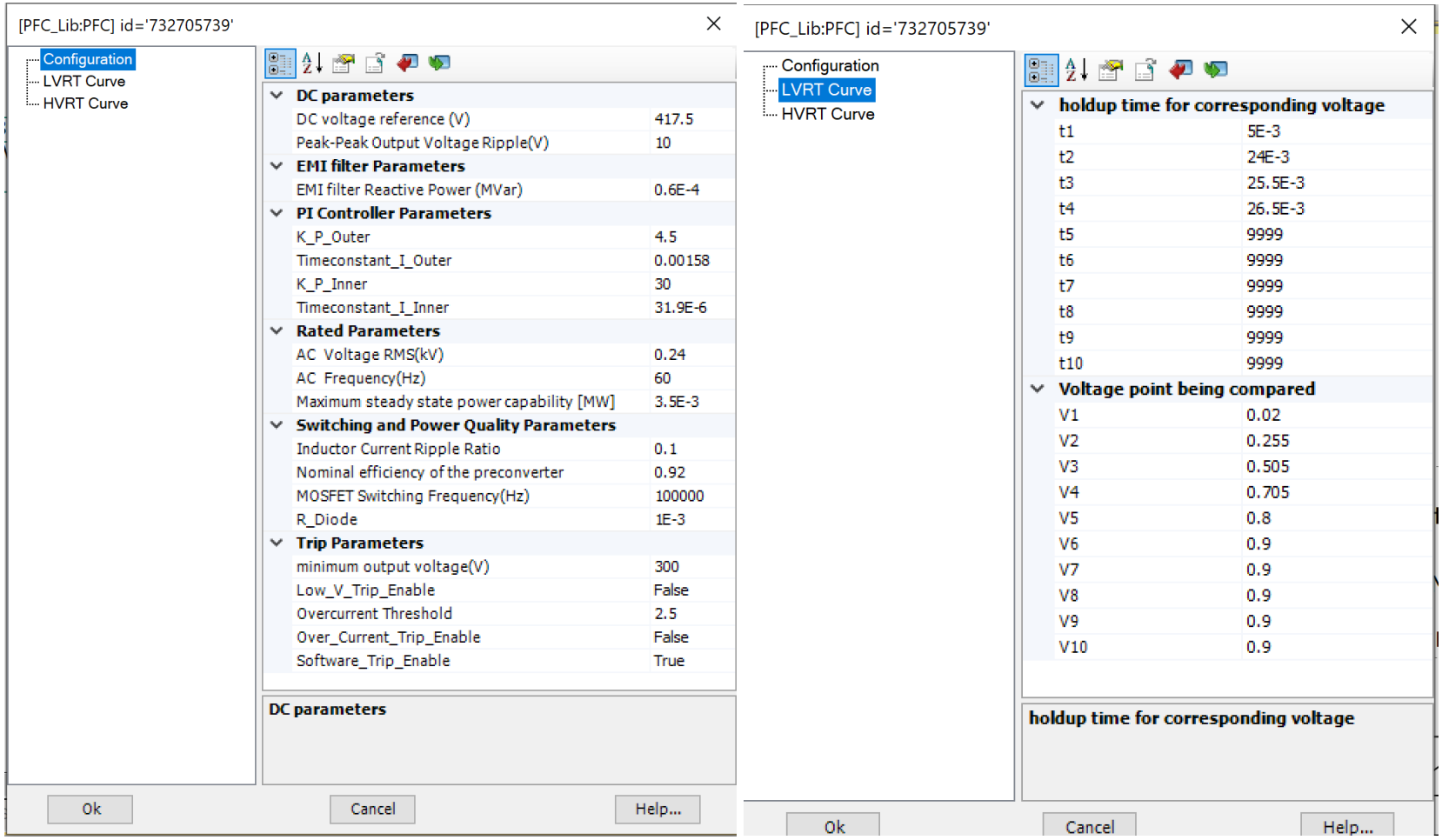


Figure 26: PSCAD parameters for model validation.

4.1. 168V (70%) sag for 2 cycles (Trip)

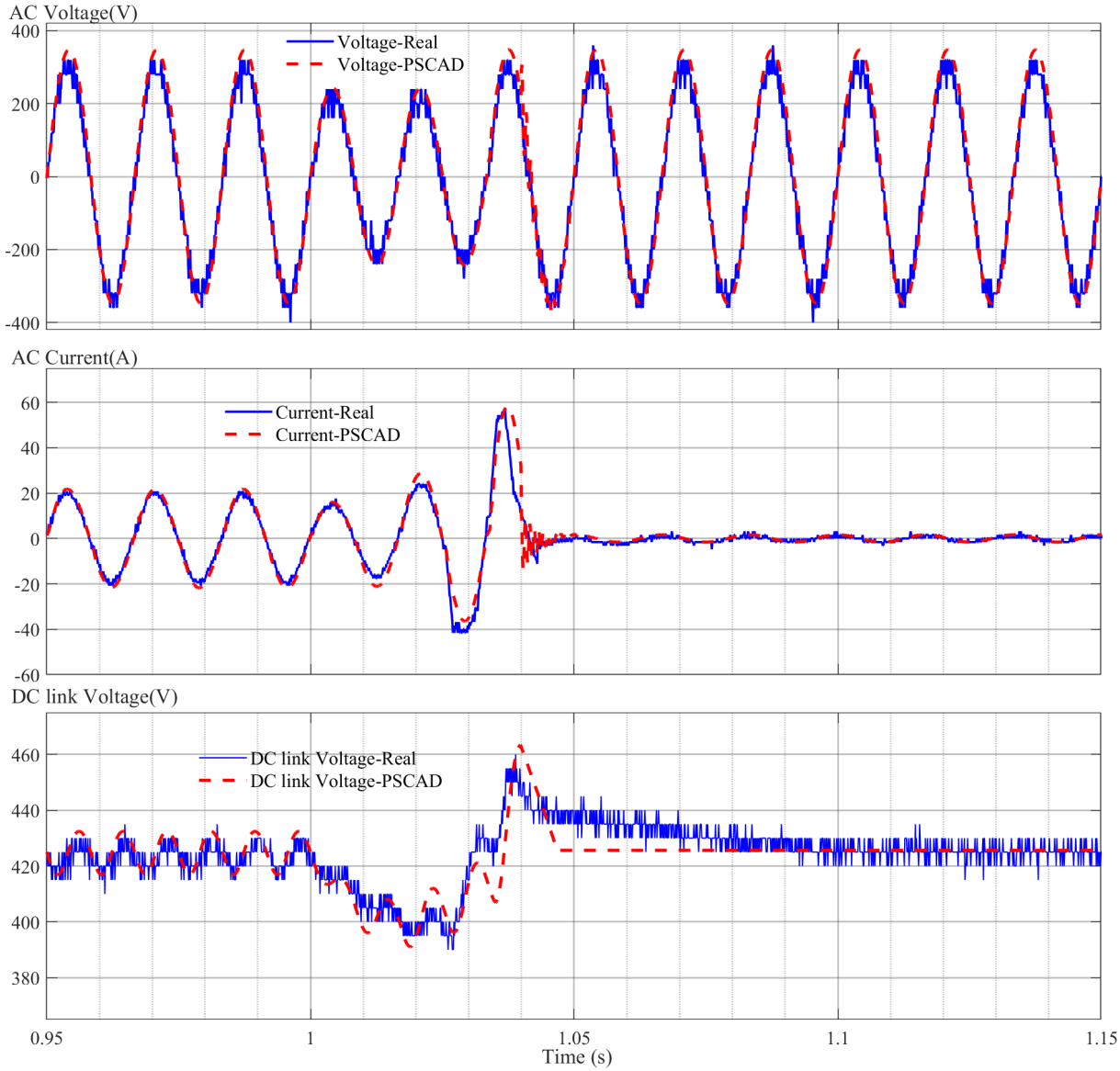


Figure 27: Voltage sags to 70% for 2 cycles. (Blue solid lines are real lab test results and red dotted lines are PSCAD results).

4.2. 175V (73%) sag (continuous operation)

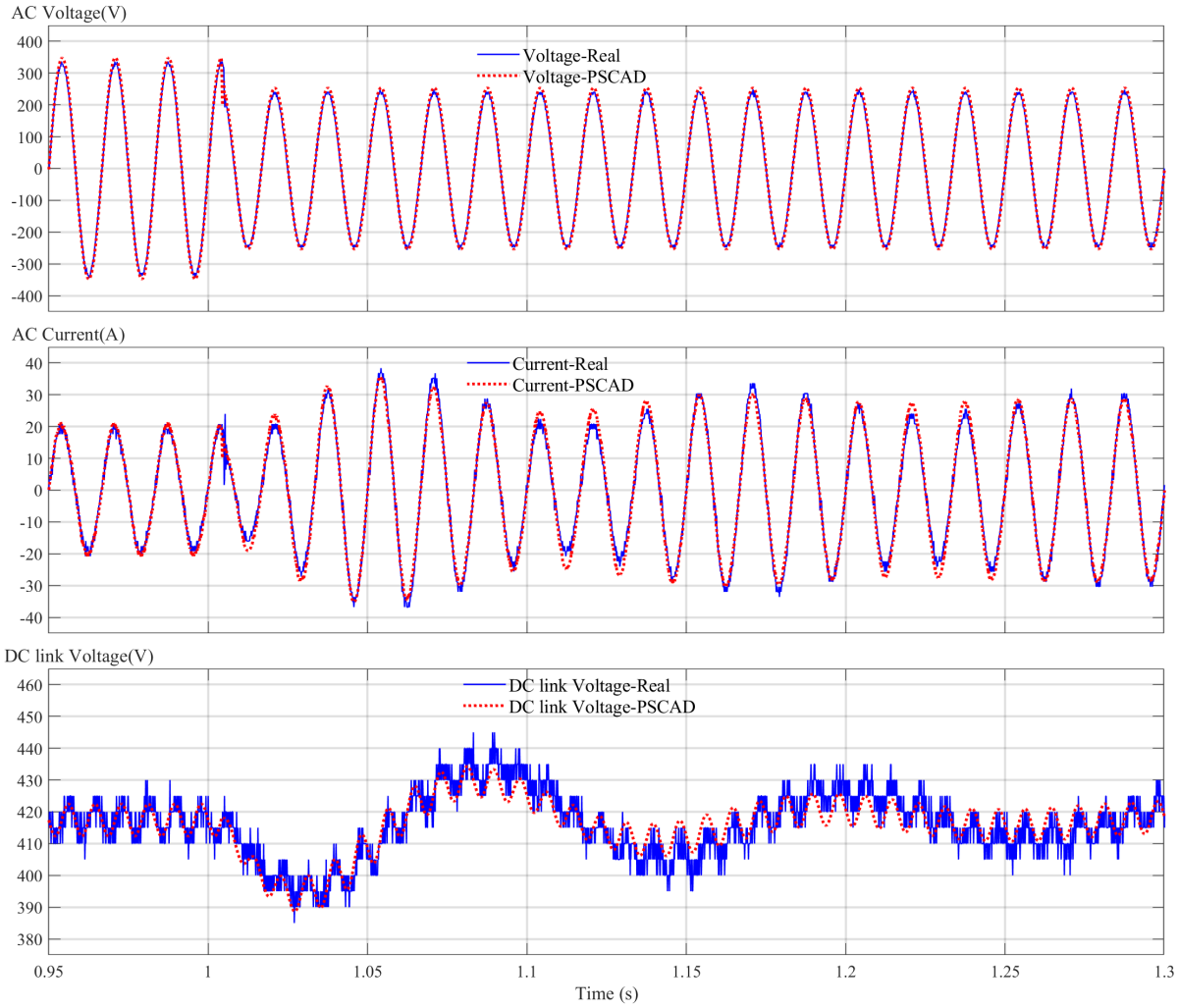


Figure 28: Voltage sags to 73% for 300ms (continuous operation.) (Blue solid lines are real lab test results and red dotted lines are PSCAD results) .

5. Small-Signal Impedance Test via Frequency Scanning

In this section, the input impedance of the developed model is tested based on frequency scanning method.

5.1. Input Impedance test method

In this subsection, we examine the small-signal frequency response of the PSCAD model, as shown in Figure 30. The input impedance is measured by injecting a small-signal disturbance voltage of magnitude V_d at frequency f, and observing the resulting current magnitude I_d at that frequency. The small signal impedance at this frequency is calculated as:

$$Z_f = \frac{V_d}{I_d} \tag{5.1}$$

For the theorical derivation, see [2].

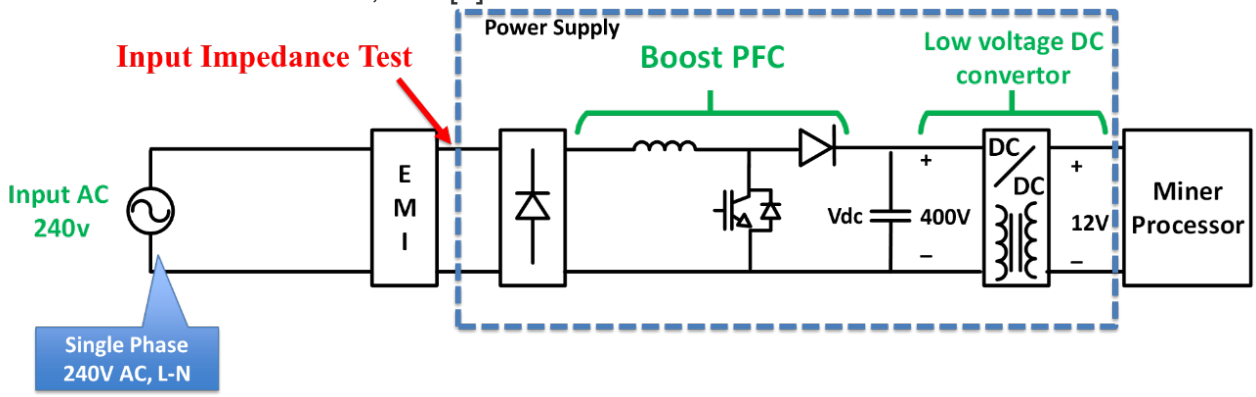


Figure 29: Input Impedance Test.

Both the average model and the switching model are tested in PSCAD using the method illustrated in Figure 31. A small-signal voltage of 2 V is injected. The load consists of a 3.3 kW resistor (48 ohm) corresponding to an equivalent AC-side resistance of 17.28 ohm. The input current is measured, and FFT analysis is performed to extract the current component at the same frequency as the injected disturbance. The disturbance frequency is swept from 5 to 50 Hz in 1 Hz steps. Each test runs for 3 s, and the steady-state current magnitude and phase at each frequency are recorded. The input impedance is then calculated according to (5.1).

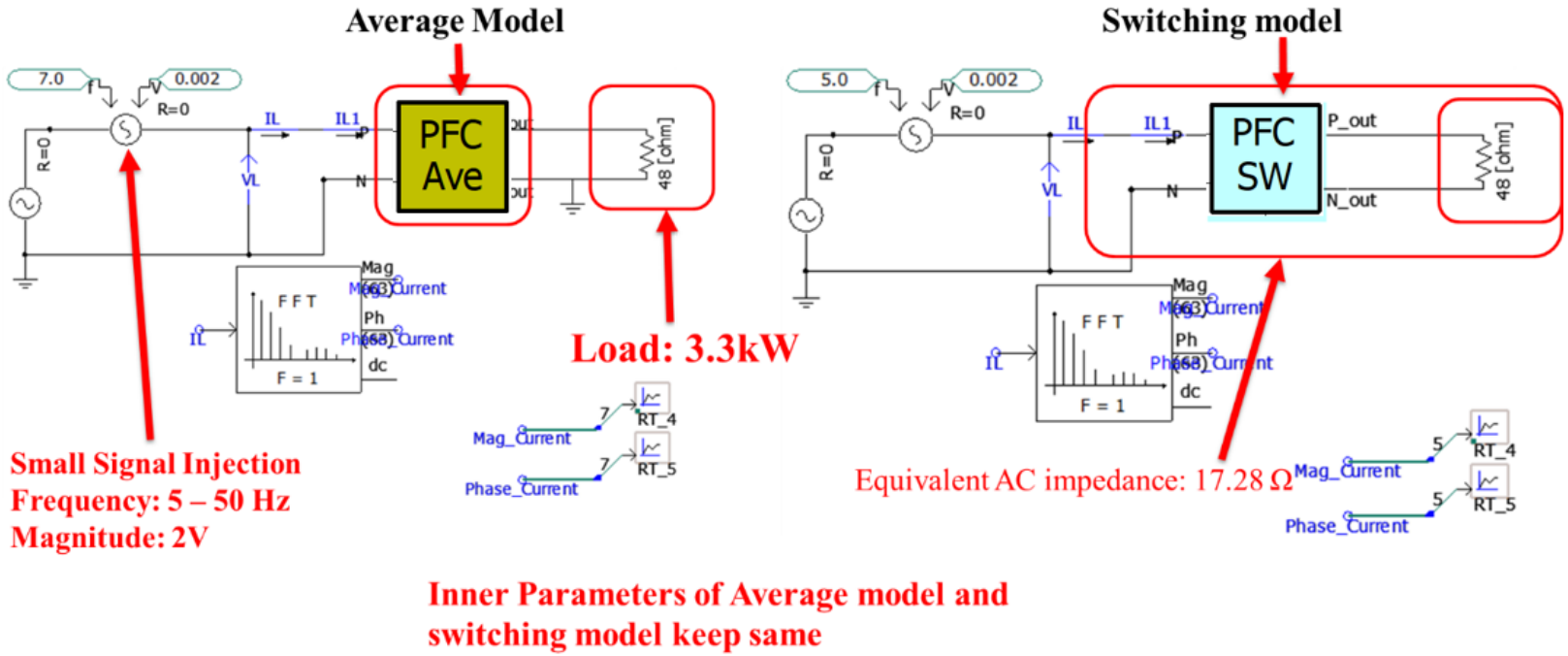


Figure 30: Input Impedance test method.

5.2. Input Impedance Test Result

The test results for the average and switching models are shown in Figure 32 and Figure 33. The input impedance of the average model closely matches that of the switching model at low frequencies, as the two models are equivalent in this range.

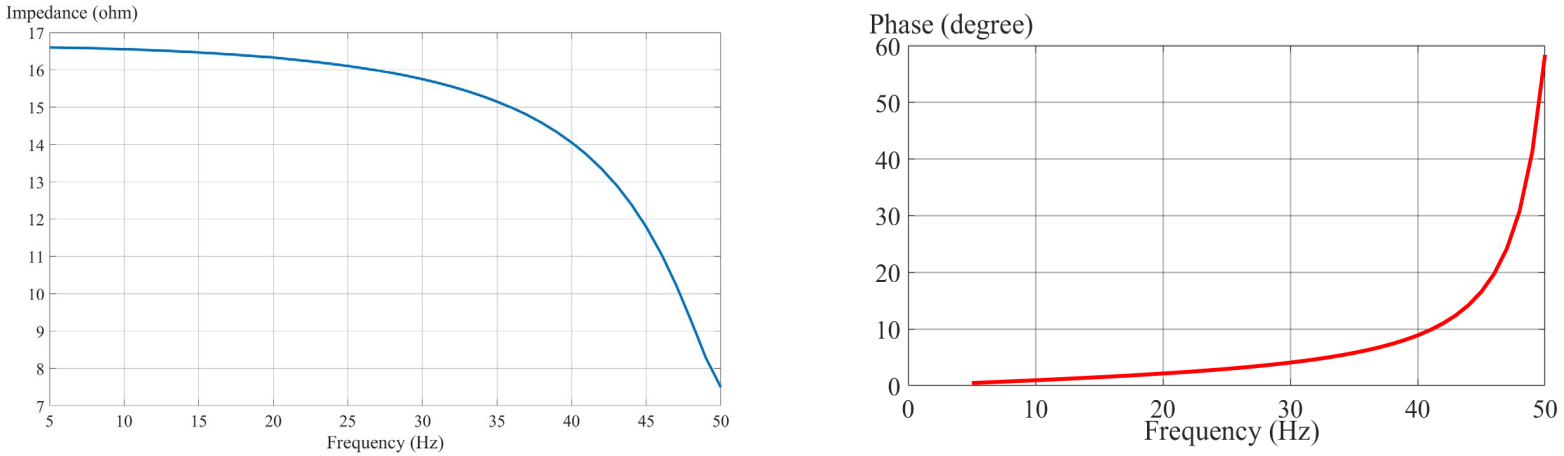


Figure 31: Input Impedance Test result of average model.

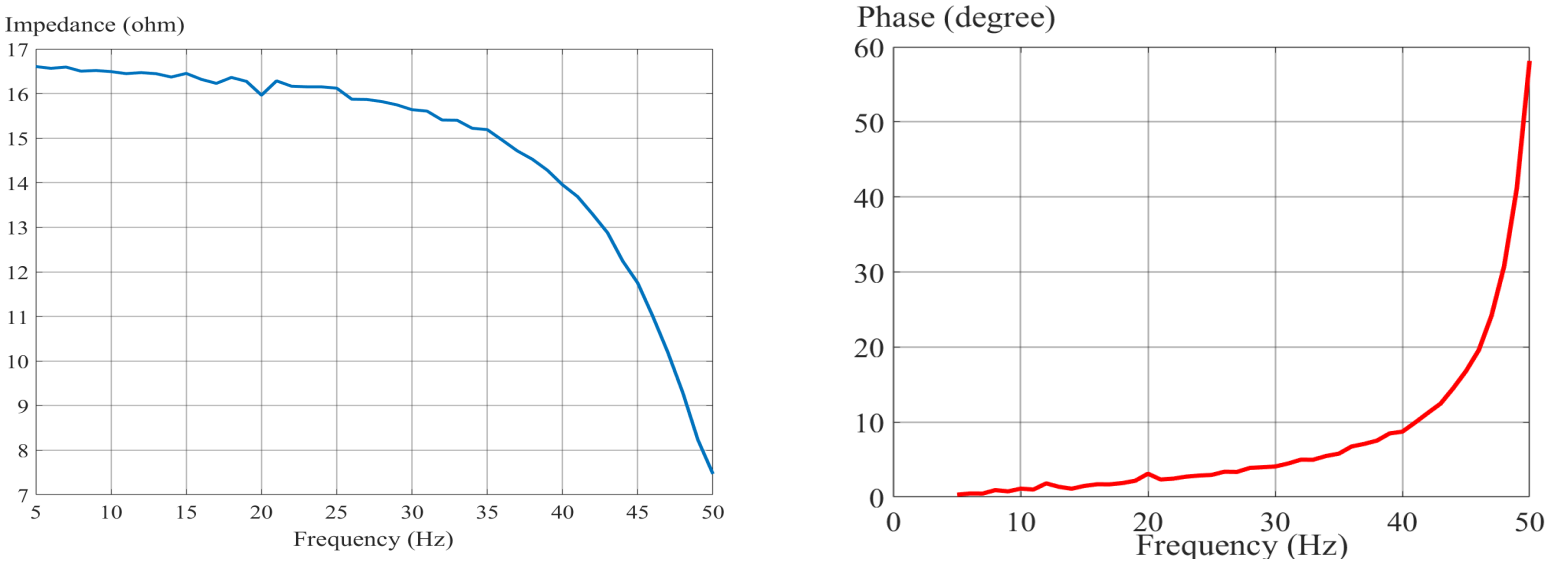


Figure 32: Input Impedance Test result of switching model.

The input impedance of the switching model is also tested over the range of 5 Hz to 2000 Hz, with results shown in Figure 34. Two resonance points are observed at 50 Hz and 70 Hz, consistent with the findings in [2] as illustrated in Figure 35. For details on the location of these resonance points, refer to the small-signal impedance model in [2].

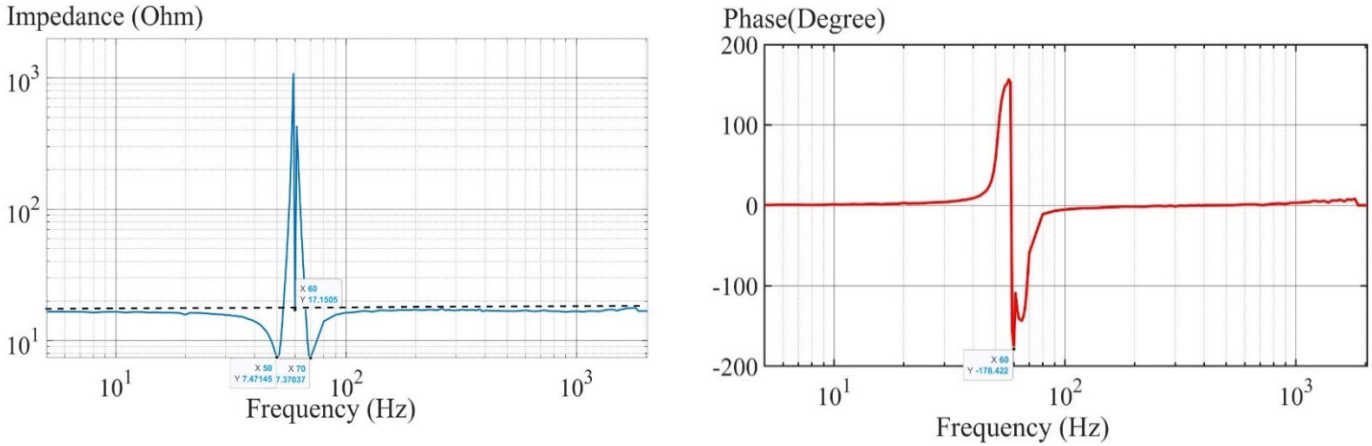


Figure 33: Input impedance test result of switch model (5Hz to 2000Hz).

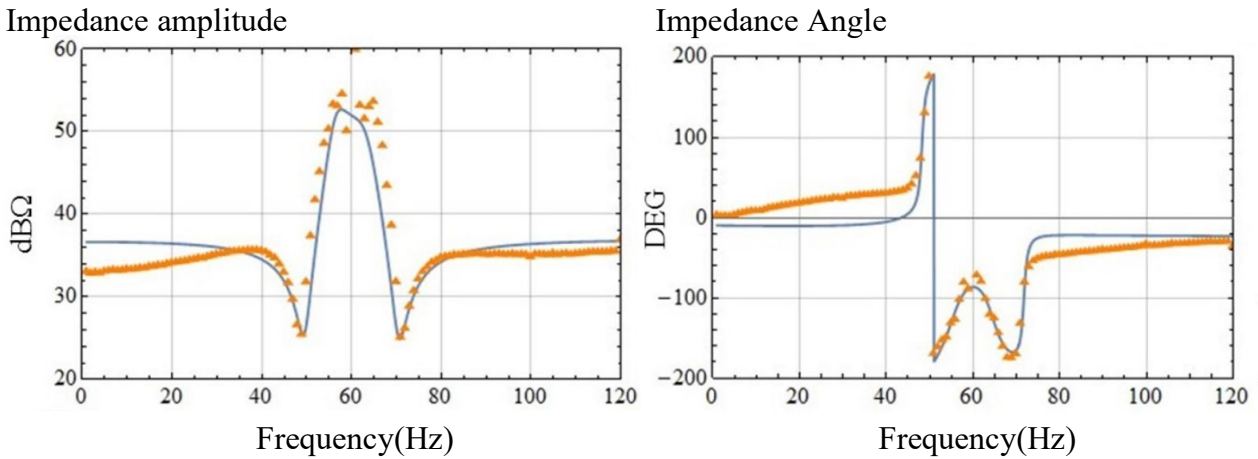


Figure 34 : Input Impedance of PFC in [2].

6. Device-Level and Facility-Level Test Case

In this section, the developed switching and average models of the crypto-miner load are tested in PSCAD using two scenarios. At the device level, a 3.5 kW crypto-miner load is connected to a 240 V AC grid, and both load disturbances and grid voltage sags are applied. The dynamic responses of the switching and average models are compared under these conditions. At the facility level, a 1 MW crypto-miner load is modeled per phase, resulting in a total three-phase load of 3 MW. This load is then scaled to 300 MW and connected to a 138 kV grid via two transformers. During load fluctuations, the dynamics are recorded and compared between the switching and average models.

6.1. Device-Level Test and Comparison between Switching model and Average model.

6.1.1.Test Electrical Circuit

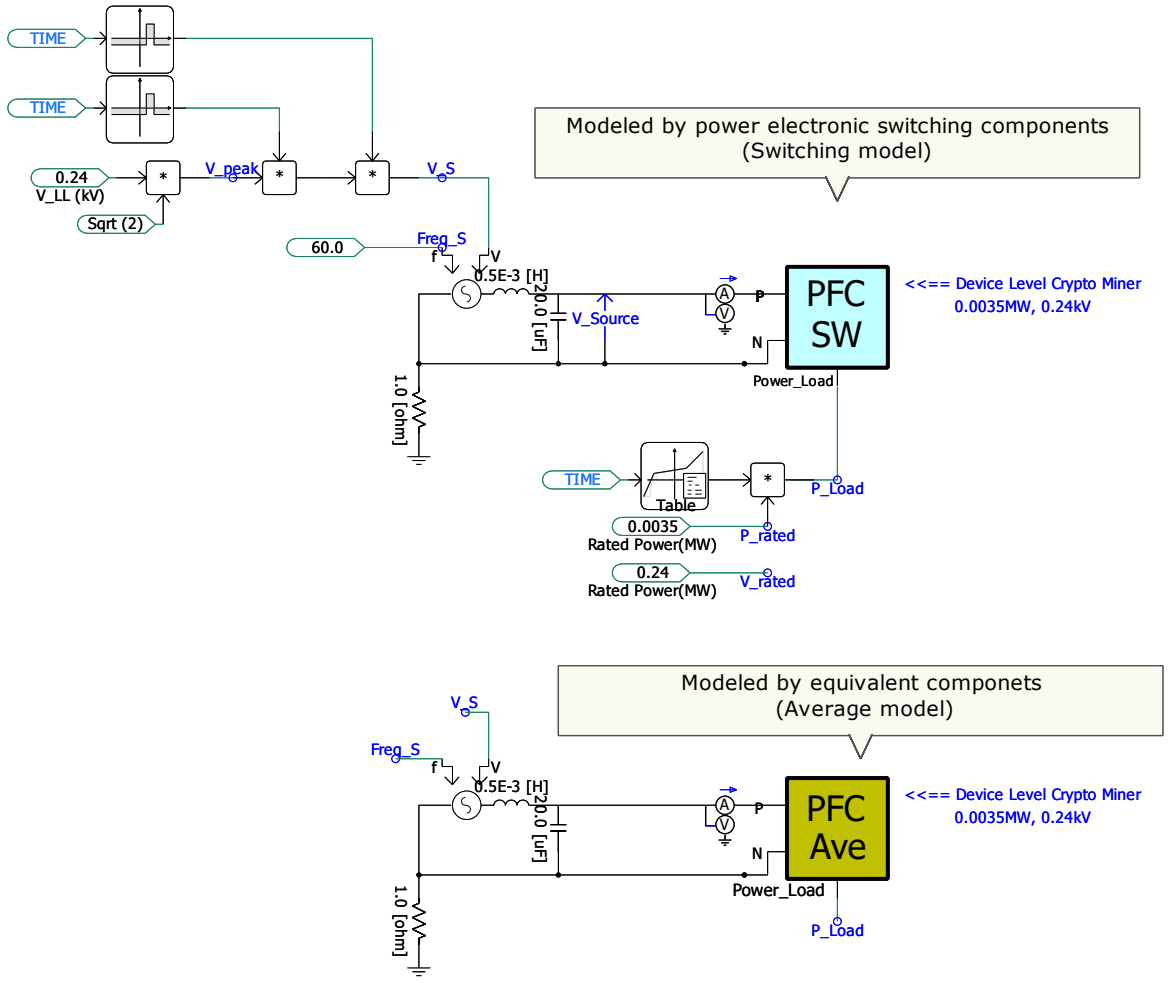


Figure 35: Device Level Test Case.

This case is included in **"CryptoMiner_Ave_SW_models"**. The electrical circuits are shown in Figure 36. Both the switching and average models are configured with a capacity of 3.5 kW and a rated AC voltage of 240 V. At 1.5 s, the AC voltage drops to

75% for 0.5 s and recovers at 2.0 s. At 2.5 s, the voltage drops to 55% for 24 ms and recovers at 2.524 s. At 3 s, the load decreases from 1 p.u. (3.5 kW) to 0.5 p.u. (1.75 kW) over 0.1 s.

The parameters of switching model and average model are set as shown in Figure 37.

DC parameters	
DC voltage reference (V)	417.5
Peak-Peak Output Voltage Ripple(V)	10
EMI filter Parameters	
EMI filter Reactive Power (MVar)	0.00016
PI Controller Parameters	
K_P_Outer	4.5
Timeconstant_I_Outer	0.00158
K_P_Inner	30
Timeconstant_I_Inner	31.9E-6
Rated Parameters	
Maximum steady state power capability [MW]	P_rated
AC Voltage RMS(kV)	V_rated
AC Frequency(Hz)	60
Switching and Power Quality Parameters	
Inductor Current Ripple Ratio	0.1
Nominal efficiency of the preconverter	0.92
MOSFET Switching Frequency(Hz)	10000
R_Diode	1E-3
Trip Parameters	
minimum output voltage(V)	300
Overcurrent Threshold	2.5
Over Voltage Trip enabled (=1) disabled (=0)	0
Over Current Trip enabled (=1) disabled (=0)	0
VRT Curve enabled (=1) disabled (=0)	1
Time delay to activate the trip settings(s)	0.2

(a) Switching Model

DC parameters	
DC voltage reference (V)	417.5
Peak-Peak Output Voltage Rippl	10
EMI filter Parameters	
EMI filter reactive power (MVar)	0.00016
PI Controller Parameters	
K_P_Outer	4.5
Timeconstant_I_Outer	0.00158
K_P_Inner	30
Timeconstant_I_Inner	31.9e-6
Rated Parameters	
Maximum steady state power ca	P_rated
AC Voltage RMS(kV)	V_rated
AC Frequency(Hz)	60
Switching and Power Quality Parameters	
Inductor Current Ripple	0.1
MOSFET Switching Frequency(H:	10000
Nominal efficiency of the precor	0.92
R_Diode	5e-3
Trip Parameters	
minimum output voltage(V)	300
OverCurrentThreshold (pu)	2.5
Over Voltage Trip enabled (=1)	0
Over Current Trip enabled (=1)	0
VRT Curve enabled (=1) disable	1
Time delay to activate the trip s	0.2

(b) Average Model

Figure 36: Parameters configuration for the test case.

P_rated is set to be 0.0035 MW and V_rated is set to be 0.24 kV. Since the EMI filter is capacitive, its reactive power is set to 160 W.

6.1.2.Test Result

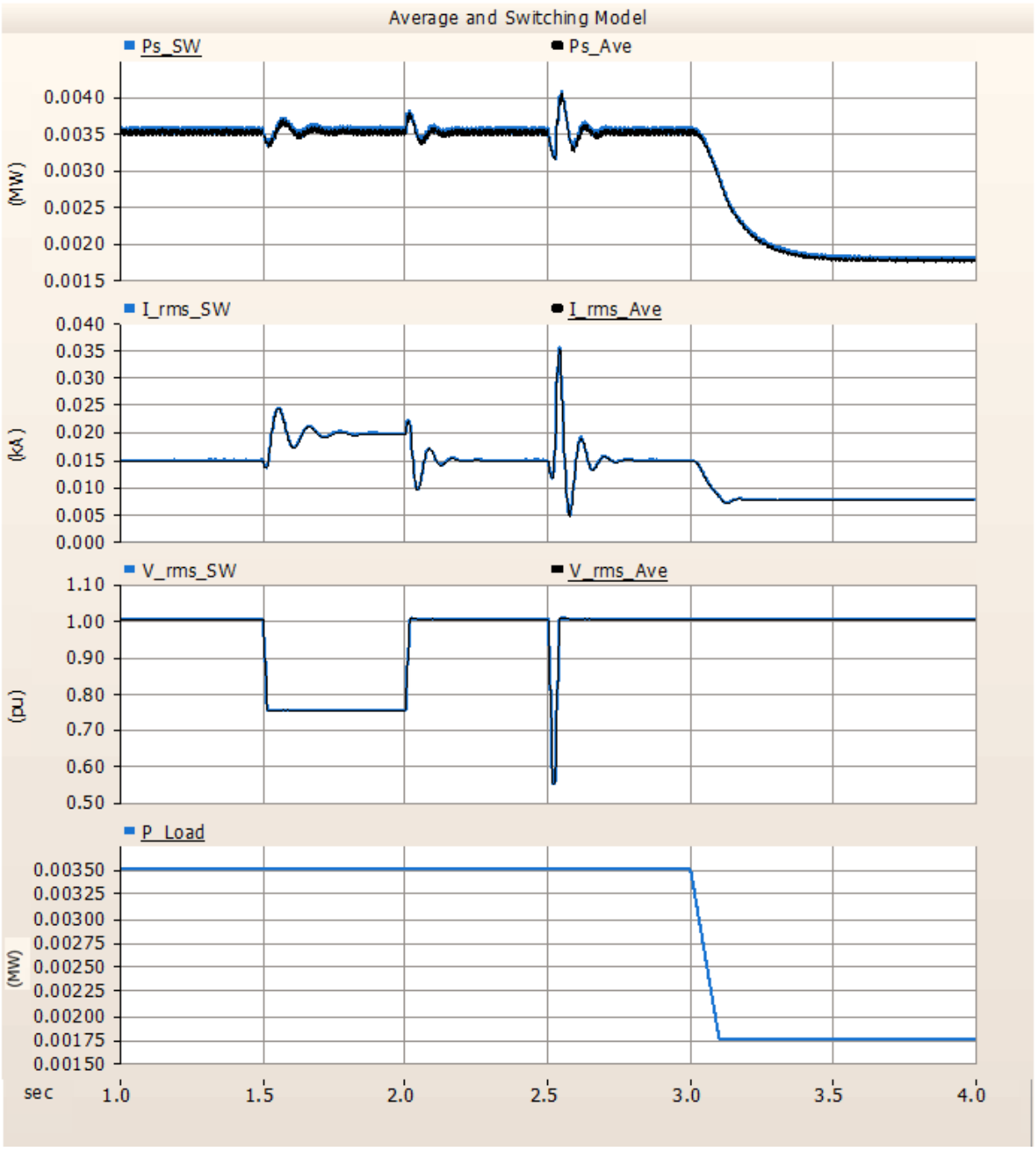


Figure 37: Device level test result: AC power (Ps_SW for switching model and Ps_Ave for average model), Current (RMS value, I_rms_SW for switching model and I_rms_Ave for average model), Voltage (RMS value, V_rms_SW for switching model and V_rms_Ave for average model.) and Computing Load (DC side constant power load P_Load).

The grid-side results are shown in Figure 38 indicating good agreement between the switching and average models. Both models show slightly higher AC power than the setpoints on the DC-side constant load. This discrepancy is due to losses in the diodes, IGBT, and large resistors in parallel with the DC-link capacitor.

The DC-link voltage for both the switching and average models is shown in Figure 39 demonstrating close agreement between the two models.

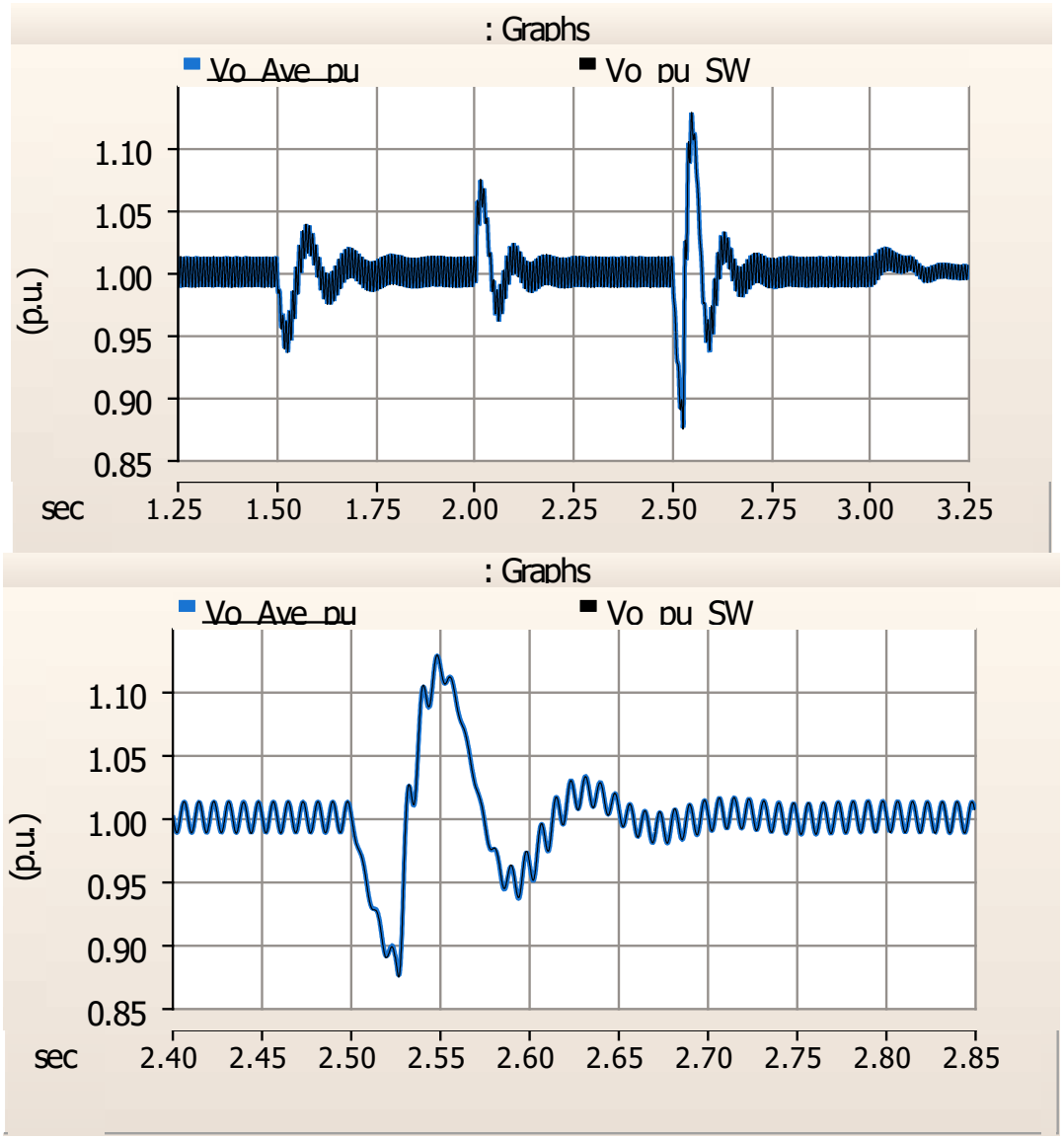


Figure 38: DC link voltage of switching model and average model. (Vo is the DC link voltage in per unit value and the base value is 400 V, the figure below is a zoomed-in view of the figure above.)

6.2. Facility Level Test Case

6.2.1.Test Electrical Circuit

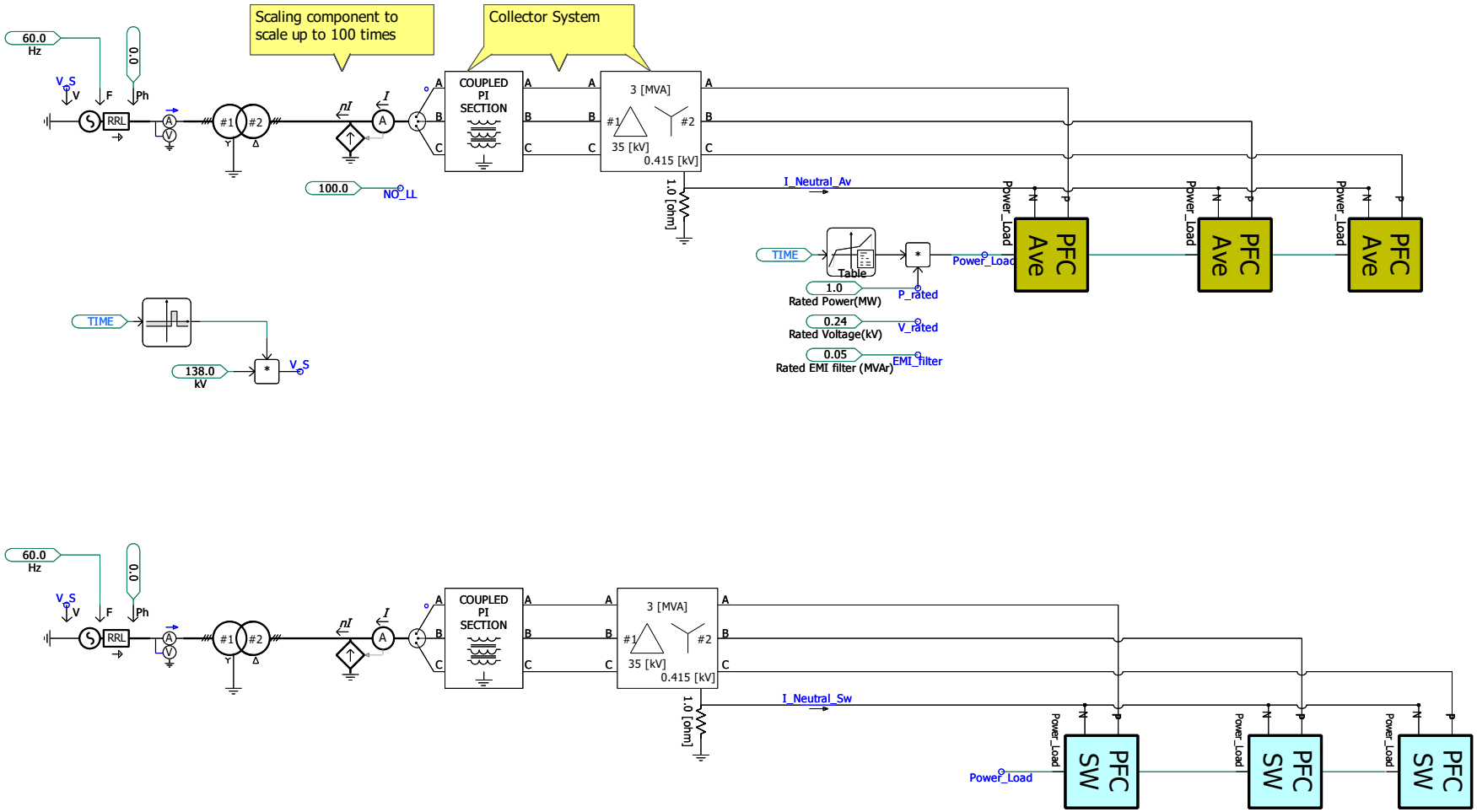


Figure 39: Facility Level Test case.

In this case, the crypto-miner model is configured with a capacity of 1 MW per phase at 240 V, yielding a total three-phase load of 3 MW. This 3 MW load is connected to the collector system, which includes a 3 MVA, 35 kV/0.45 kV transformer and a π-type transmission line. A scaling component with a factor of 100 is then applied to scale the power to 300 MW, which is connected to a 300 MVA, 138 kV/35 kV transformer and ultimately tied to the grid. The test case electrical circuit is shown in Figure 40.

6.2.2.Test results

The load increases from 0 to 75 MW (0.75 p.u.) at t=0s over 0.5 s, and then further ramps from 75 MW to 300 MW (3 p.u.) at t=3s over 0.1 s. At 5s, the voltage in 138kV side drops to 80% and recovers to 138kV at 5.5s. The voltage, active power, and reactive power responses are shown in Figure 41. The active power of the switching model closely matches that of the average model, while a slight difference in reactive power occurs due to 10 kHz switching harmonics, which introduce additional reactive power losses in the two transformers. At 5 s, when the voltage drops to 80%, the current increases from 3 p.u. to 3.75 p.u. to maintain constant DC power, resulting in higher reactive power losses in the transformers.

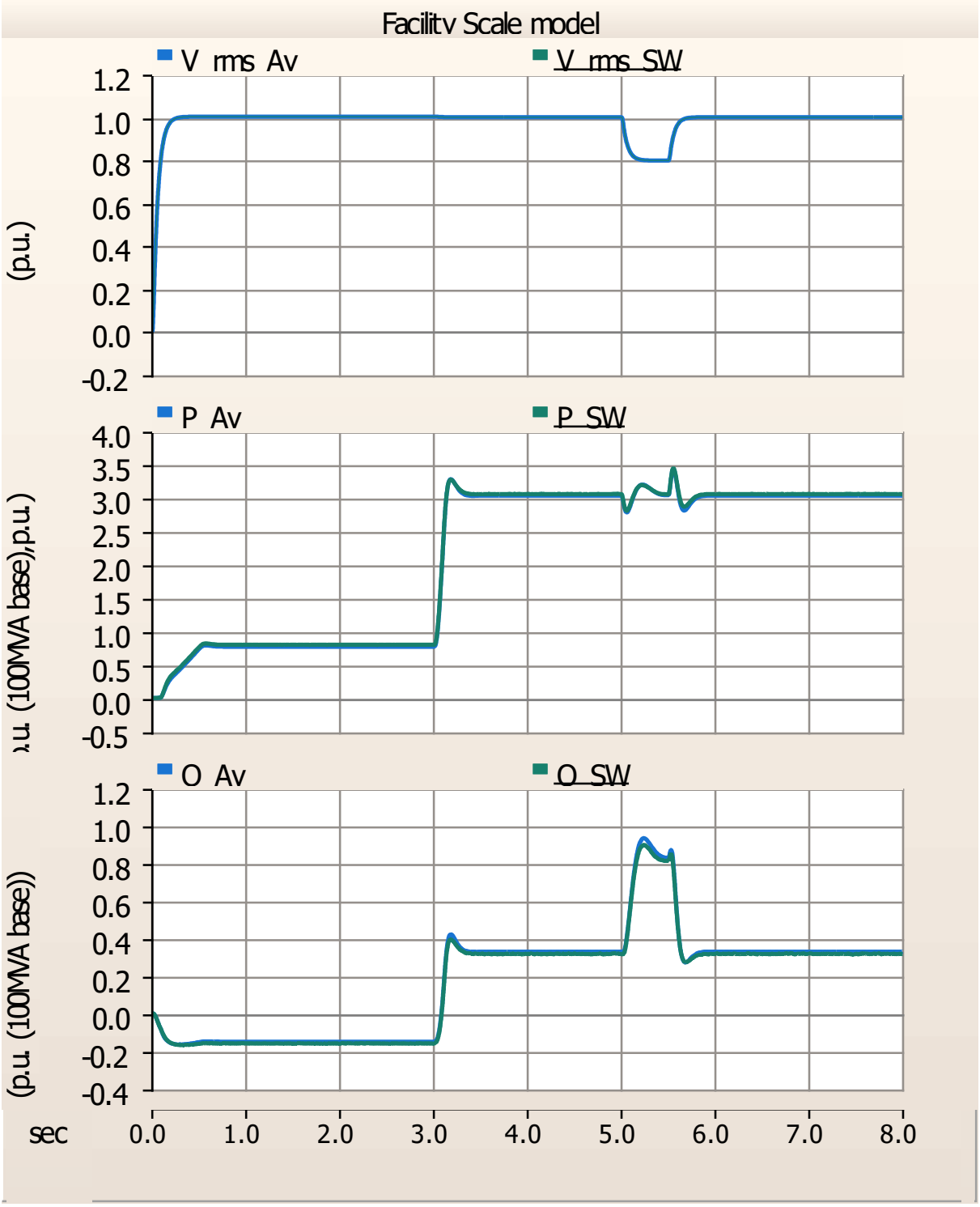


Figure 40: Facility Level Test Result. (P_Av and P_SW are the 138kV AC side active power. Q_Av and Q_SW are the 138kV side reactive power. The base value is 100MVA. V_rms_Av and V_rms_SW are the RMS voltage in 138kV side.)

7. Reference

[1] L. Bao, L. Fan and Z. Miao, "Modeling and Analysis of Single-phase Boost Converter with Power Factor Correction Control," 2020 52nd North American Power Symposium (NAPS), Tempe, AZ, USA, 2021, pp. 1-6.

[2] J. Sun, M. Xu, M. Cespedes and M. Kauffman, "Low-Frequency Input Impedance Modeling of Single-Phase PFC Converters for Data Center Power System Stability Studies," *2019 IEEE Energy Conversion Congress and Exposition (ECCE)*, Baltimore, MD, USA, 2019, pp. 97-106

[3] M. Chen and J. Sun, "Low-Frequency Input Impedance Modeling of Boost Single-Phase PFC Converters," in *IEEE Transactions on Power Electronics*, vol. 22, no. 4, pp. 1402-1409, July 2007

[4] Toshiba Electronic Devices & Storage Corporation. “Power Factor Correction (PFC) Circuits Application Note.” 2019. https://toshiba.semicon-storage.com/info/docget.jsp?did=68570