Dynamic Modeling of Crypto-Miner Load in PSCAD

Version 1.0

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Open-Source Model Link

Large Load Modeling

Suggested Citation

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Summary

The report develops and validates open-source electromagnetic transient (EMT) models in PSCAD to represent crypto-miner loads for use in transmission-level stability analysis and large electronic load studies. The models capture the essential behavior of crypto-mining equipment through a power factor correction (PFC)-based front-end converter and a constant-power computing load.

Validation against a 3.5 kW crypto-miner device shows that the models accurately reproduce low-voltage ride-through behavior, transient current response, DC-link voltage dynamics, and protection actions during voltage disturbances. The close match between simulation and laboratory measurements confirms the fidelity of the models at the device level.

To support transmission-system studies, the models incorporate voltage ride-through characteristics aligned with the Electric Reliability Council of Texas (ERCOT)'s Large Electronic Load Ride-Through Requirements, including DC-link undervoltage protection, overcurrent protection, and configurable low-voltage ride-through (LVRT) and high-voltage ride-through (HVRT) curves. Frequency-domain analysis further verifies that the models capture the low-frequency impedance characteristics important for subsynchronous oscillation analysis for power-system stability.

Both switching and average-value model implementations are provided. Comparisons show that the average model preserves the key dynamic characteristics of the detailed switching model while significantly reducing computational burden, making it suitable for large-scale EMT simulations of crypto-mining facilities.

Overall, the models offer a practical and validated framework for analyzing the impact of large-scale crypto-mining facilities on power-system dynamics, voltage stability, and ride-through performance, and they can also be applied to subsynchronous oscillation studies in modern power grids.

Table of Contents

Abbreviations

AC	Alternating Current
Ave	Average
DC	Direct Current
EMI	Electromagnetic Interference
EMT	Electromagnetic Transient
HVRT	High-Voltage Ride-Through
IGBT	Insulated-Gate Bipolar Transistor
LC	Inductor-Capacitor
LVRT	Low-Voltage Ride-Through
PFC	Power Factor Correction
PI	Proportional-Integral
PSCAD	Power Systems Computer Aided Design
p.u.	Per Unit
PWM	Pulse Width Modulation
RMS	Root Mean Square
SR	Set-Reset
SW	Switching
VRT	Voltage Ride-Through

1. Introduction

The rapid growth of large-scale crypto-mining facilities and their sensitivity to voltage disturbances have raised concerns regarding grid stability. To better understand these impacts and support transmission reliability studies, it is essential to develop accurate electromagnetic transient (EMT) models that can effectively capture their voltage-dependent dynamic behavior.

To investigate these effects, this project develops open-source EMT simulation models of crypto-mining loads in power systems computer aided design (PSCAD). The developed models provide the following key features and insights:

1. The crypto-miner load is modeled as a power factor correction (PFC) circuit connected to a constant power load.
2. Both switching (SW) and average (Ave) models are developed. The average model omits high frequency switching to improve computational efficiency, allowing users to choose between higher accuracy or faster simulation speed depending on the study scope. Both models are benchmarked with each other, and the results are consistent.
3. The model includes DC-link low-voltage and over-current protection schemes.
4. The voltage ride-through (VRT) characteristic can be additionally defined to account for both low-voltage ride-through (LVRT) and high-voltage ride-through (HVRT) trip conditions that are not captured by DC link low-voltage and over-current protection.
5. The PSCAD models were benchmarked against laboratory test results for the device-level model. The benchmarked device-level model was then used to develop the facility-level model for the crypto-mining load.

Table 1 provides an overview of the open-source PSCAD files and their functions.

Table 1: File list and functionality of the open-source PSCAD model.

File name	File functionality
CryptoMiner_PSCADmodel_Ws.pswx	**PSCAD workspace**. It defines the locations of all required files. Opening this workspace automatically loads all libraries and test cases.
Crypto_Miner_Library.pslx	**PSCAD library**. It contains both the average and switching modules used in the test cases. This library must be added to the workspace before use.
CryptoMiner_Ave_SW_models.pscx	**Device-level test case.** The switching and average models, each rated at 3.5 kW, are evaluated under identical operating conditions, and their dynamic responses are compared. The detailed results are presented in Section 6.1.
CryptoMiner_SW_Ave_Facility.pscx	**Facility-level test case.** The switching and average models, each rated at 1MW per phase, are evaluated under identical operating conditions, and their dynamic responses are compared. The detailed results are presented in Section 6.2.

The remainder of this report is organized as follows: Section 2 introduces the switching and average models of the crypto-miner load in PSCAD. Section 3 describes the operation scheme of the PFC circuit and its voltage and current controllers. Section 4 discusses the model validation by comparing simulated and laboratory results for LVRT. Section 5 presents impedance analysis results for both average and switching models. Section 6 provides comparison results at the device level (3.5 kW) and facility level (300 MW). Finally, Section 7 gives a conclusion for this report.

2. Modules and Components Description

In this section, we present the PSCAD implementation of the crypto-miner model. The crypto-miner is represented in the EMT domain as a PFC circuit connected to a constant power load. Both switching and average models are developed in PSCAD to support simulations with different accuracy and computational requirements.

2.1. Crypto-Miner Switching Model

2.1.1. Graphic

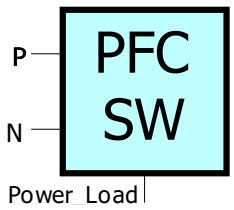

Figure 1: Graphic of switching model.

The graphic of the crypto-miner switching model is shown in Figure 1. The model includes two electrical input terminals, namely the single-phase AC live wire (P) and neutral wire (N). The control input port, “Power_Load”, represents the real-time computing power demand of the crypto-miner load.

2.1.2. Parameters

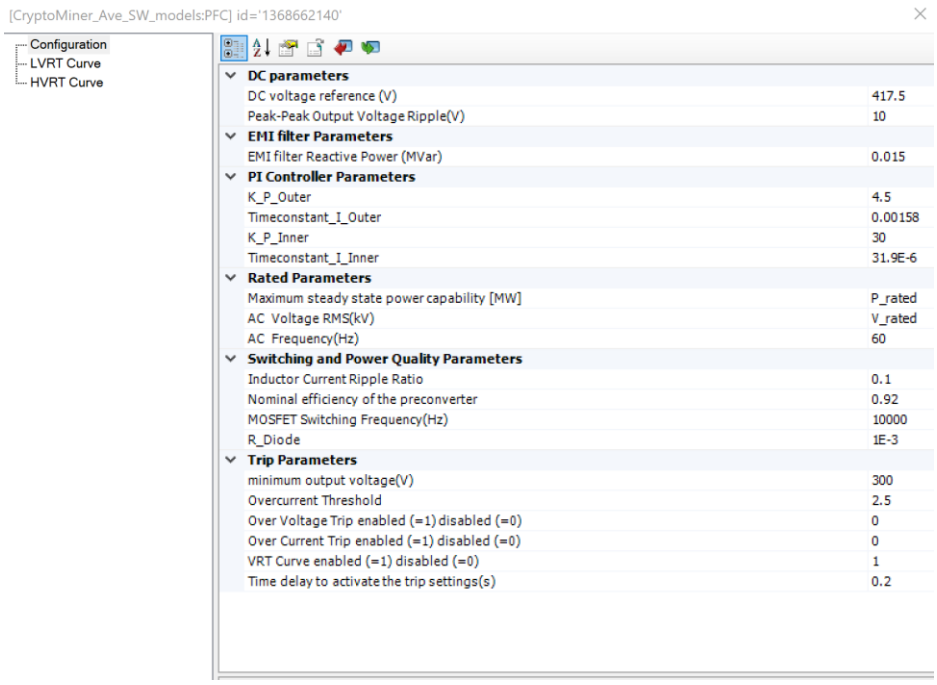

Figure 2: Parameters of the switching model.

The model parameters are shown in Figure 2, including the rated AC and DC operating parameters, electromagnetic interference filter (EMI) filter reactive power settings, proportional-integral (PI) controller parameters, switching and power quality parameters, and trip protection settings.

Note that “R_Diode” represents the equivalent resistance of the five diodes used in the switching model and is typically set to a small value, such as 0.1% of the equivalent load impedance. When VRT curve-based trip detection is enabled, both the LVRT and HVRT curves must be specified, as illustrated in Figure 3. The corresponding LVRT and HVRT curve parameters are shown in Figure 4, where each curve is specified by a series of voltage thresholds and the associated ride-through durations.

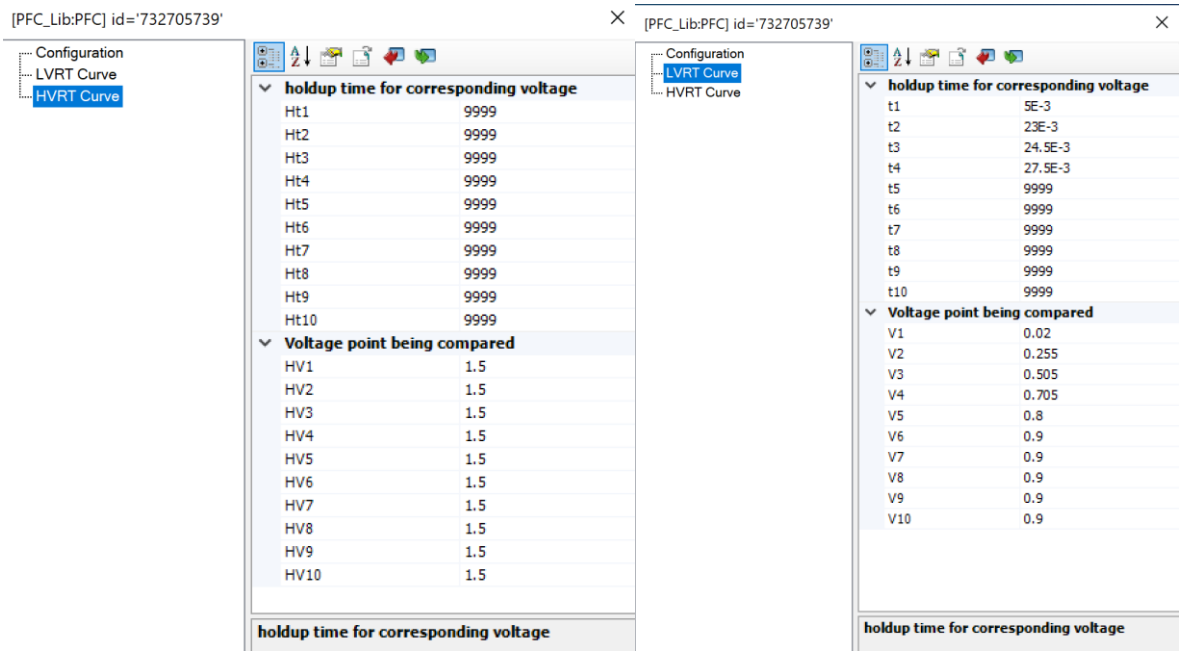

Figure 3: LVRT curve and HVRT curve.

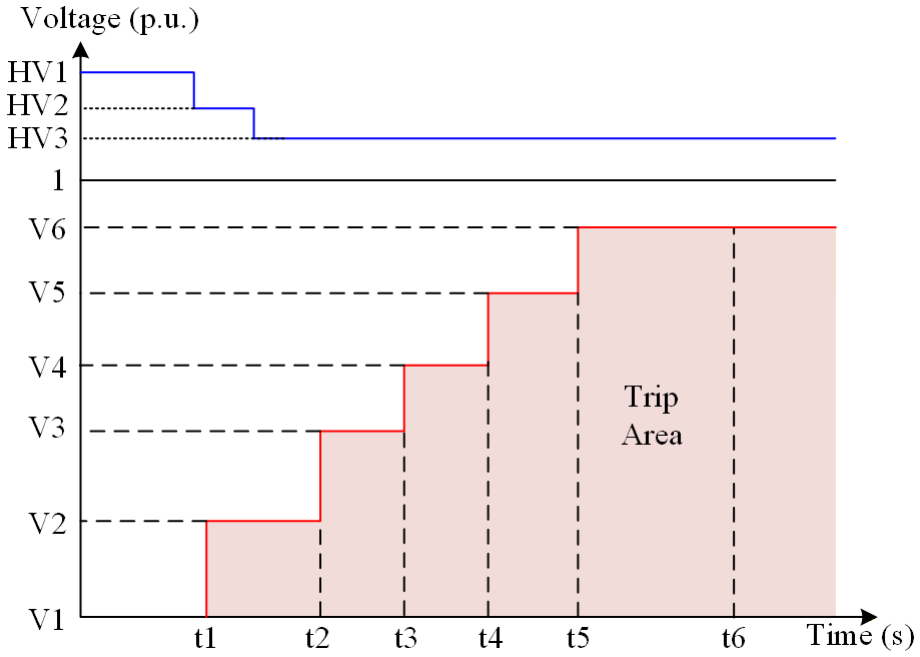

Figure 4: Illustrations of VRT curve (Here, only 6 points in LVRT and 3 points of HVRT are added; in the model, up to 10 points can be added for both LVRT and HVRT).

2.1.3. Model Definition

Figure 5 presents the overall schematic of the model, which includes the main power circuit, outer voltage and inner current controllers, constant power load control, protection functions, the VRT mechanism, inductor-capacitor (LC) parameter calculation modules, and sections for signal monitoring and visualization.

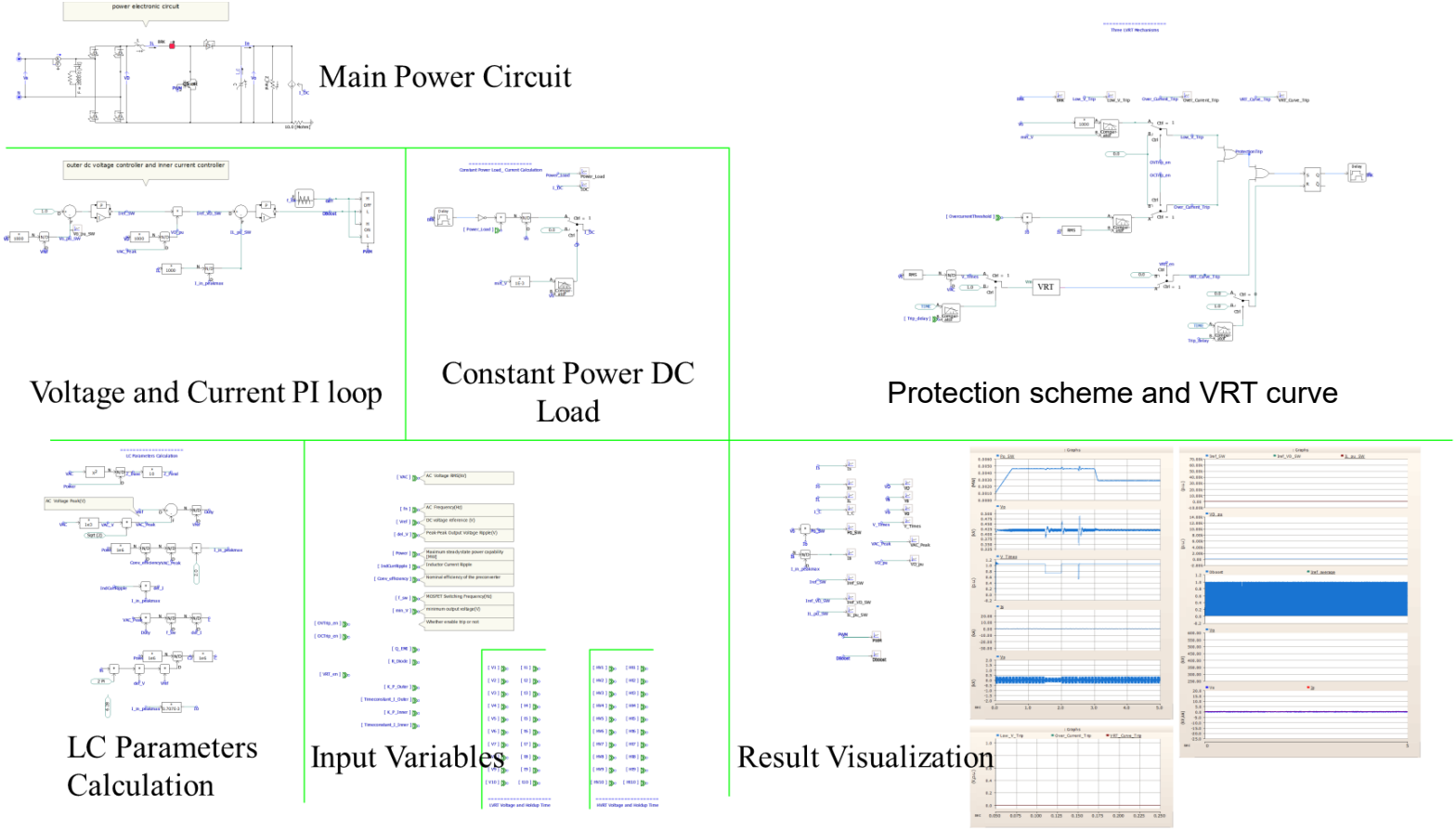

Figure 5: Overview of switching model schematics. (The average model is almost the same.).

2.1.3.1. Main Power Circuit

The main power circuit of the crypto-miner is the power factor correction (PFC) circuit, as shown in Figure 6. The input voltage passes through the EMI filter (capacitive filters), followed by the rectifier and the boost circuit. A virtual breaker (ideal switch) is inserted to emulate the trip mechanism.

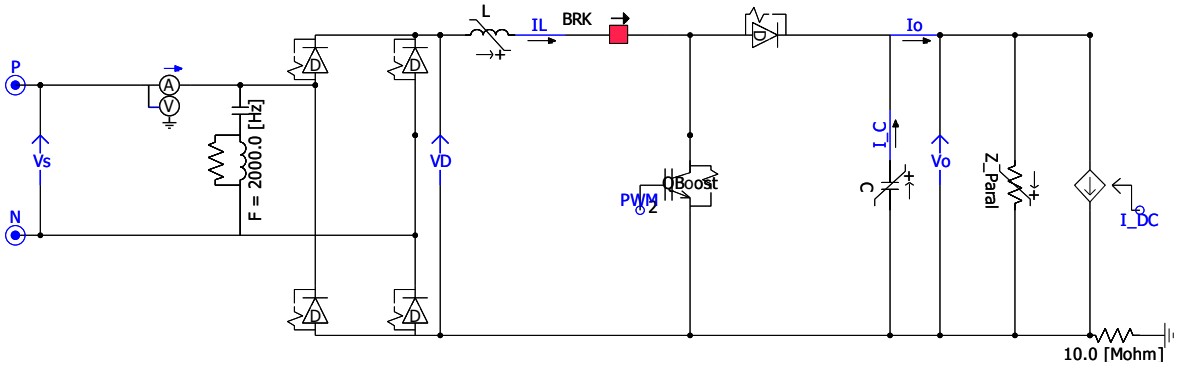

Figure 6: Definition of the switching model.

2.1.3.2. LC Parameters Calculation

The LC parameters are calculated automatically based on the rated power, voltage, and current ripple, and DC voltage ripple, as shown in Figure 7.

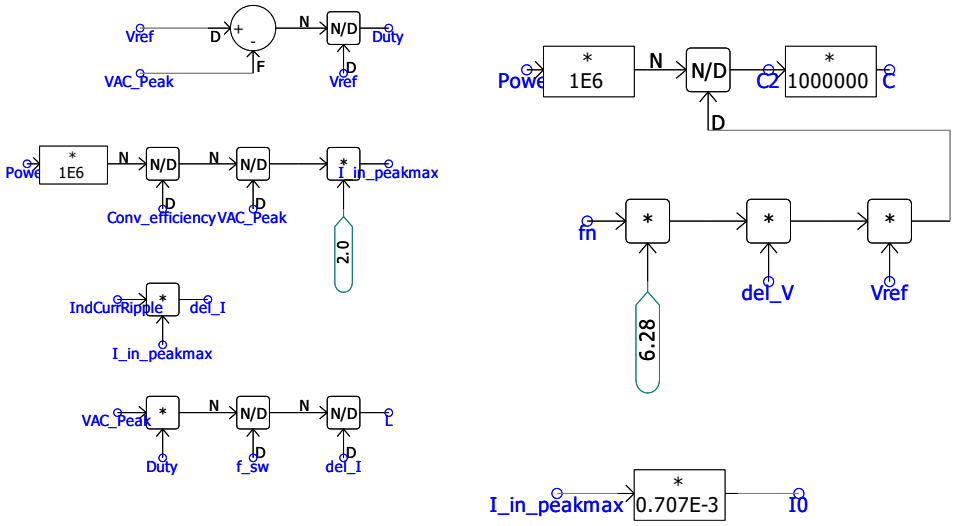

Figure 7: LC parameters calculation.

The nominal duty ratio at the peak input voltage is calculated as:

$$D = \frac{V_o - V_{\text{AC\_max}}}{V_o}, \tag{2.1}$$

where V_o denotes the output DC voltage. $V_{\text{AC\_max}}$ denotes the input AC peak voltage.

The nominal duty ratio represents the converter operating point under rated conditions, while the instantaneous duty ratio varies with the rectified AC voltage and contains both the 120 Hz low-frequency component and the high-frequency pulse width modulation (PWM) switching components.

The input current is calculated as:

$$I_{\text{AC\_max}} = \frac{2P_o}{\eta V_{\text{AC\_max}}}, \tag{2.2}$$

where η denotes the efficiency and P_o denotes the rated output power.

The inductor AC current ripple:

$$\Delta I_L = \Delta I_{L,p} \times I_{\text{AC\_max}}, \tag{2.3}$$

where $\Delta I_{L,p}$ is the inductor current ripple ratio, as defined in the model parameters.

The inductor and capacitor values are then calculated as follows:

$$L = \frac{V_{\text{AC\_max}} \times D}{\Delta I_L f_{\text{sw}}}, \tag{2.4}$$

$$C = \frac{P_o}{V_o \times \Delta V_o \times 2\pi f_n}, \tag{2.5}$$

where f_{sw} is the switching frequency, ΔV_o is the peak-peak output voltage ripple, specified by the user, and f_n denotes the grid frequency, which is set to 60 Hz in the model.

2.1.3.3. Voltage Loop and Current Loop PI Controller

The PI controllers, as shown in Figure 8 are designed based on per-unit values. The parameters of the outer-loop and inner-loop PIs can be adjusted in the model's configuration settings. The output of the current loop is the duty of the boost switching insulated-gate bipolar transistor (IGBT). Finally, the duty is used to generate the PWM wave based on the carrier frequency.

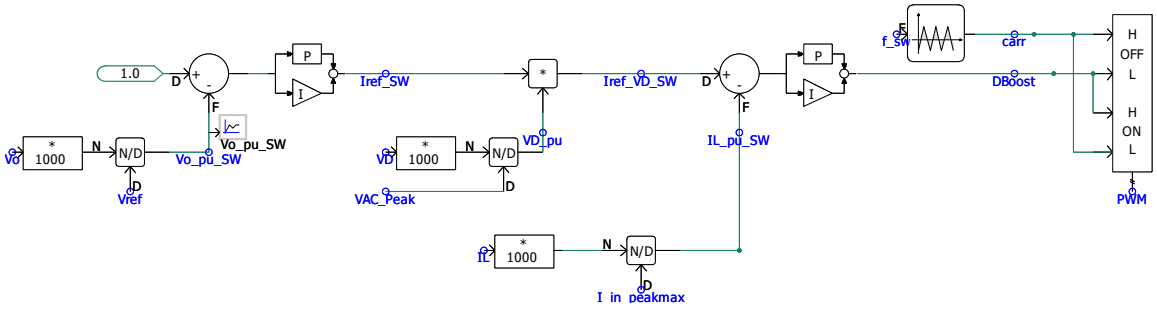

Figure 8: Controller of the PFC circuit, including the outer voltage loop, inner current loop, and PWM generator.

2.1.3.4. Constant-Power Computing Load

The constant power load is used to represent the computing load of the crypto-miner. During transient events, the computing load is assumed to behave as a constant power load. The constant power load is implemented using a controlled current source, as shown in Figure 9. The current "I_DC" is calculated as:

$$I_{\mathrm{DC}} = \frac{P \times BRK}{\max\{V_{\mathrm{DC}}, 10^{-3}\}}, \tag{2.6}$$

where BRK denotes the binary trip signal. When a trip occurs, the constant power load is disconnected, and its power consumption is set to zero.

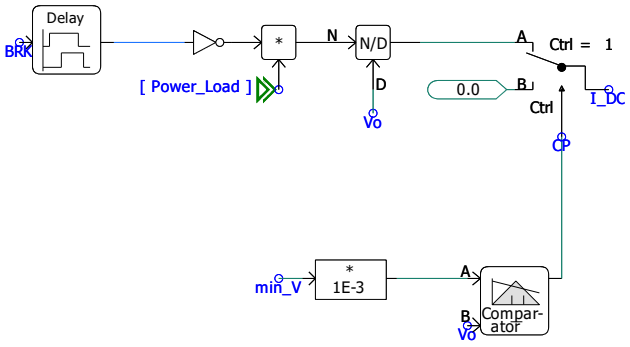

Figure 9: Constant Power Load model, which is used to model the DC computing load of the crypto-miner.

2.1.3.5. Voltage Ride-Through Trip Mechanism

There are three types of VRT trip mechanisms, as shown in Figure 10. The trip signal passes through a set-reset (SR) flip-flop and will remain latched until the trip condition is manually reset.

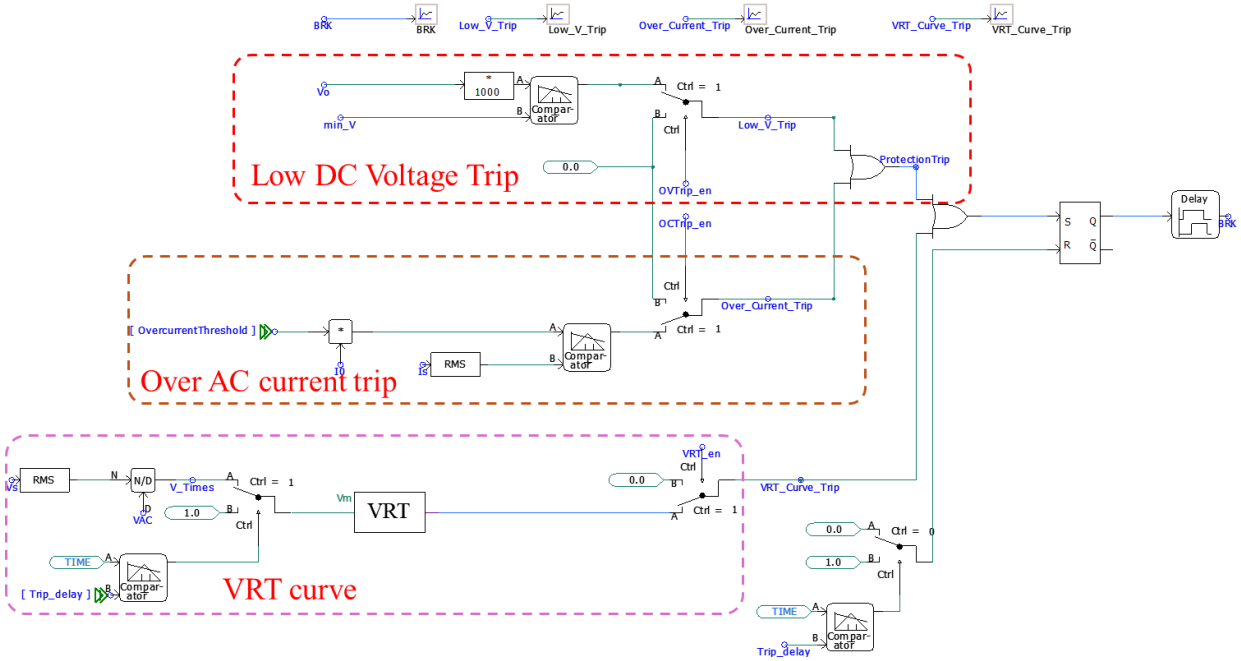

Figure 10: Protection settings and the VRT curve mechanisms.

1) Low DC voltage trip

   The DC-link voltage is continuously monitored. A trip signal is issued when the DC voltage falls below the minimum threshold specified in the model parameters.

2) AC Overcurrent trip

   The root mean square (RMS) value of the AC current is measured and compared against a user-defined threshold, which is specified as a multiple of the rated current. A trip signal is generated when the measured current exceeds this threshold.

3) VRT Curve Trip Detection (LVRT Curve and HVRT Curve)

   The RMS value of the AC voltage is monitored and evaluated against the predefined LVRT and HVRT curves. A trip signal is generated if the voltage remains outside the

allowable ride-through region for longer than the corresponding ride-through duration specified by the VRT curves.

The outputs of the three protection mechanisms are combined through a logical OR operation to generate the final trip signal.

2.2. Crypto-Miner Average Model

2.2.1. Graphic

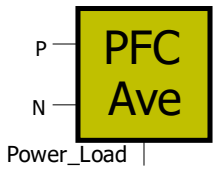

Figure 11: Graphic of PFC average model.

The graphic of the crypto-miner average model is shown in Figure 11. The model includes two electrical input terminals, namely the single-phase AC live wire (P) and neutral wire (N). The control input port, “Power_Load”, represents the real-time computing power demand of the crypto-miner load.

2.2.2. Parameters

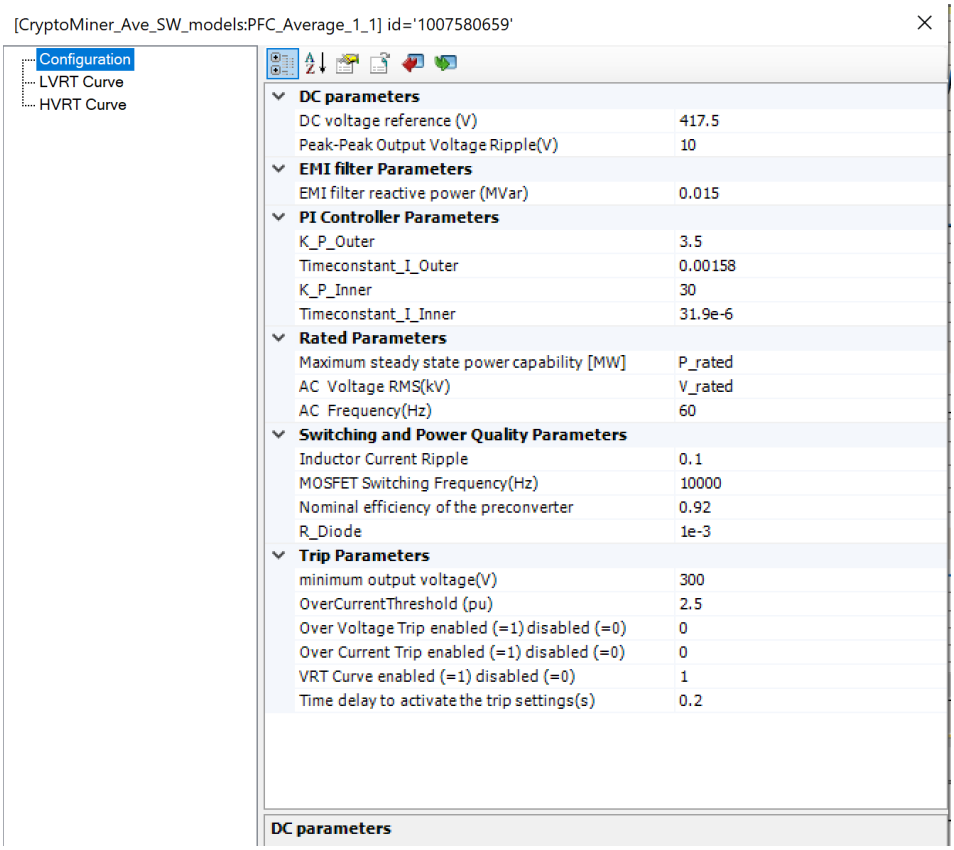

Figure 12: Parameters for the average model.

The parameters of the average model, shown in Figure 12, are largely identical to those of the switching model. In the average model, the switching frequency is used for the calculation of the inductor value and should therefore remain consistent with the value used in the switching model.

2.2.3. Model Definition

The electric circuit of the PFC average model is shown in Figure 13. In the average model, the rectifier is represented by a controlled voltage source and a controlled current source as shown in Figure 14. The voltage source is controlled according to the absolute value of the AC input voltage, while the current source follows the inductor current, with its direction determined by the polarity of the AC voltage. The switching IGBT is replaced by a controlled voltage source and a controlled current source. The voltage source connected in series with the inductor is controlled as:

$$V_{\mathrm{L}} = (1-D)V_o = D_{\mathrm{off}}V_o\,, \tag{2.7}$$

and the current source connected in parallel with the DC-link capacitor is controlled as:

$$I_C = (1-D)I_{\mathrm{L}} = D_{\mathrm{off}}I_{\mathrm{L}}\,, \tag{2.8}$$

where D is the duty ratio generated by the controller, $D_{\mathrm{off}} = 1-D$ is off-duty cycle.

For the details of the average model, see [1] for more information.

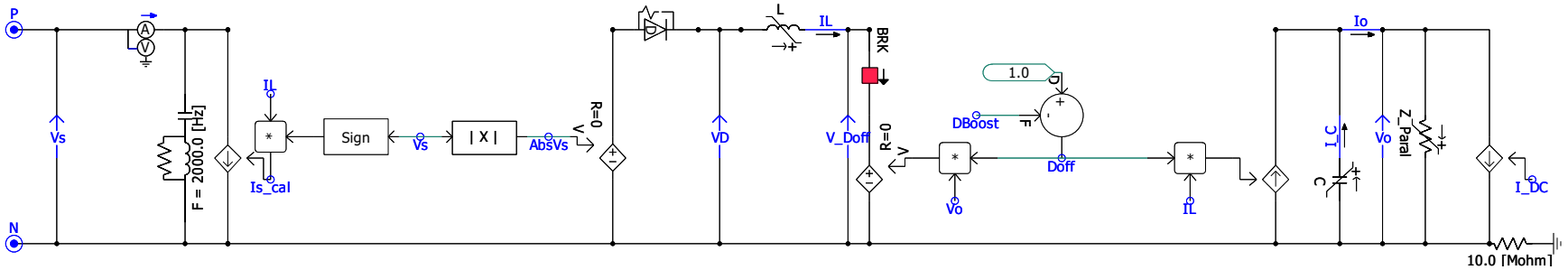

Figure 13: Model definition of average model.

The diagram of the average model is shown in Figure 14.

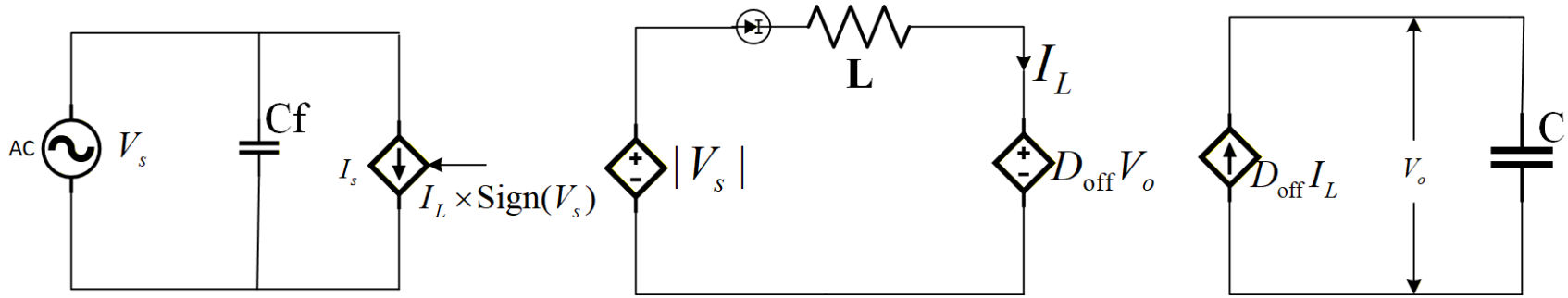

Figure 14: Diagram of the average model.

2.3. Voltage Ride-Through Curve

To accurately represent the voltage ride-through behavior of actual crypto-miners, the model includes a user-configurable VRT curve-based trip mechanism. The LVRT and HVRT curves can be customized to reproduce the ride-through characteristics of different devices. Similar VRT functions are commonly implemented in commercial crypto-miners to comply with industry standards and protection requirements, such as those curves specified by ITIC[2] and IEEE 2800-2022[3].

As shown in Figure 15, the RMS value of the AC voltage is continuously monitored and compared against a predefined voltage threshold. When the measured voltage falls below the threshold, a timer is initiated. If the voltage remains below the threshold for longer than the corresponding ride-through duration, a trip signal is generated. The VRT curve parameters are shown in Figure 16. In the current implementation, up to 10 operating points can be specified for both the LVRT and HVRT curves. Additional points can be incorporated by modifying the internal implementation of the VRT module.

Figure 15: VRT Curve-based trip detection module.

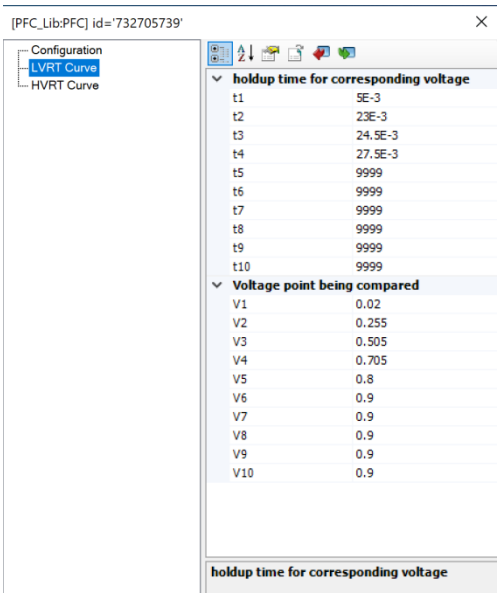

Figure 16: VRT curve parameters.

The implementation of the VRT curve-based trip mechanism is shown in Figure 17. The measured RMS AC voltage V_{m} is compared with a predefined voltage threshold V_i . When V_{m} falls below V_i , a delay timer with duration t_i is initiated. If the voltage remains below the threshold after the specified delay, a trip signal is generated. Additional operating points can be incorporated by duplicating the comparison and timing blocks within the module.

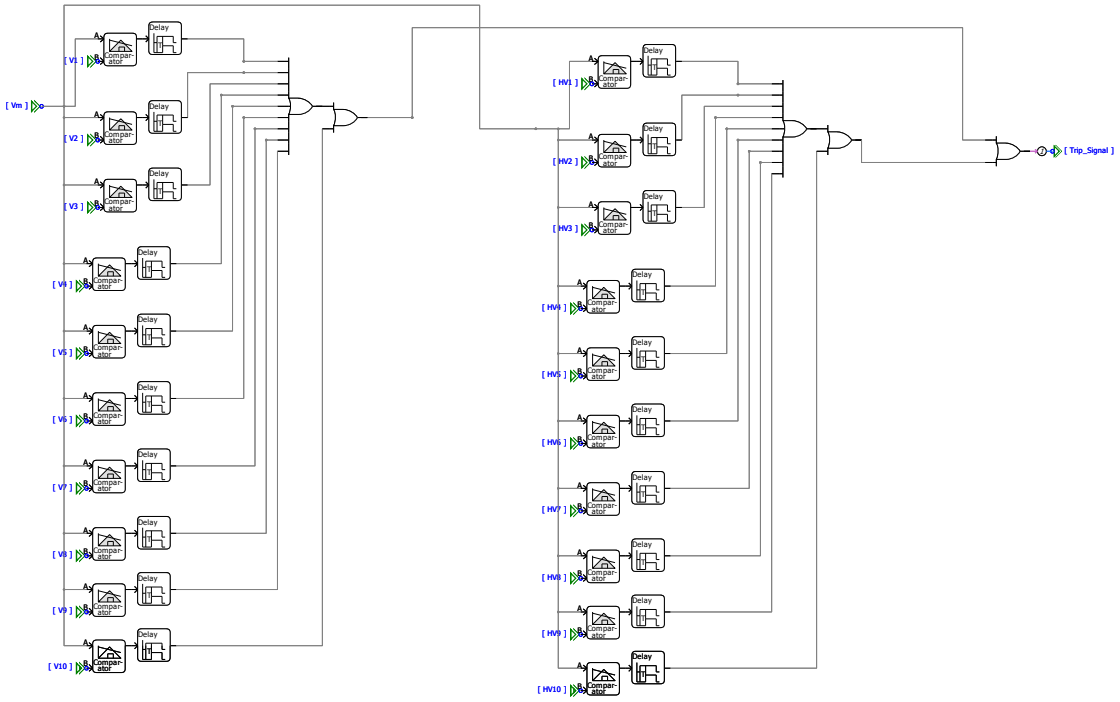

Figure 17: LVRT and HVRT curve implementation mechanism.

3. Power Factor Correction Circuit

This section describes the operation and control of the PFC circuit. First, the main electrical circuit and current flow paths are presented. Next, the dual-loop PI control structure, consisting of the outer voltage loop and inner current loop, is introduced. Finally, the effects of PI controller tuning are discussed, with particular emphasis on the trade-offs among voltage ride-through capability, transient overshoot, and system stability.

3.1. Main Electrical Circuit

Figure 6 illustrates the electrical circuit of the crypto-miner load, which consists of the following components:

1) **The diode bridge** rectifies the source voltage (V_s) into a rippled DC voltage (V_D)
2) **The boost converter** generates a smooth output voltage (V_o) across the capacitor
3) **Load** modeled as a current source and controlled to operate as a constant power load.

For the PFC circuit used in the crypto-miner, the AC source voltage, V_s is 240V AC (RMS), and the DC-link voltage V_o is around 400V, which supplies the miner's internal voltage regulation stages. The primary objective of the PFC controller is to regulate the input current such that it remains in phase with the input voltage, thereby achieving a near-unity power factor.

Unlike a full-bridge AC/DC converter, the rectification stage consists only of uncontrolled diodes. Current shaping is achieved through the IGBT in the boost converter. As illustrated in Figure 18, when the IGBT is turned on, energy is stored in the inductor as it is charged by the AC source (red path #1), while the DC-link capacitor supplies power to the load. When the IGBT is turned off, the energy stored in the inductor is released, and both the AC source and the inductor provide power to charge the DC-link capacitor and supply the load.

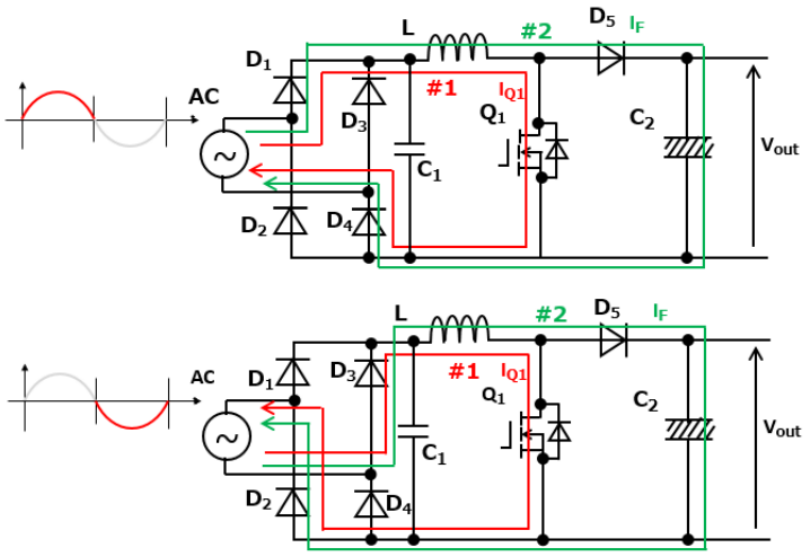

Figure 18: Current paths in the PFC circuit [4].

To regulate the DC-link voltage, the on-state and off-state durations of the boost converter IGBT must be controlled. Let D denote the duty ratio, representing the fraction of a switching period during which the IGBT is turned on. Accordingly, $1-D$ represents the fraction of the switching period during which the IGBT is turned off.

When the IGBT is turned on, the voltage at the right-hand side of the inductor is zero. When the IGBT is turned off, the voltage at the right-hand side of the inductor is equal to the DC-link voltage, V_o.

Therefore, the average voltage at the right-hand side of the inductor is:

$$(1-\bar{D})V_o. \tag{3.1}$$

Under steady-state conditions, the average voltage across the inductor must be zero according to the volt-second balance principle. Therefore,

$$(1-\bar{D})\bar{V}_o = \text{Average}(|V_{\text{AC}}|), \tag{3.2}$$

where $\bar{D}$ is the average duty, and $\text{Average}(|V_{\text{AC}}|)$ is the average rectified voltage.

3.2. Dual-Loop Control for DC Voltage Regulation and Phase Tracking

To adaptively control the output DC voltage, a voltage loop is employed, as shown in Figure 19. The input to the loop is the difference between the reference DC voltage V_{ref} (set to 1.0 in per unit (p.u.) value), and the measured output DC voltage V_o. V_{ref} is a configurable reference DC voltage, typically set to 400 V. $\frac{V_o}{V_{ref}}$ is the measured DC voltage in per unit value. The output of the voltage loop is the average reference current I_{ref_SW}. When the output DC voltage is below the reference 400 V, the inductor is charged with a larger current. The transfer function of the voltage loop is given by:

$$I_{ref\_SW} = (K_P + \frac{K_I}{s})(1 - \frac{V_o}{V_{ref}}), \tag{3.3}$$

where K_P is the outer-loop proportional gain and K_I is the outer-loop integral gain, s is the Laplace variable.

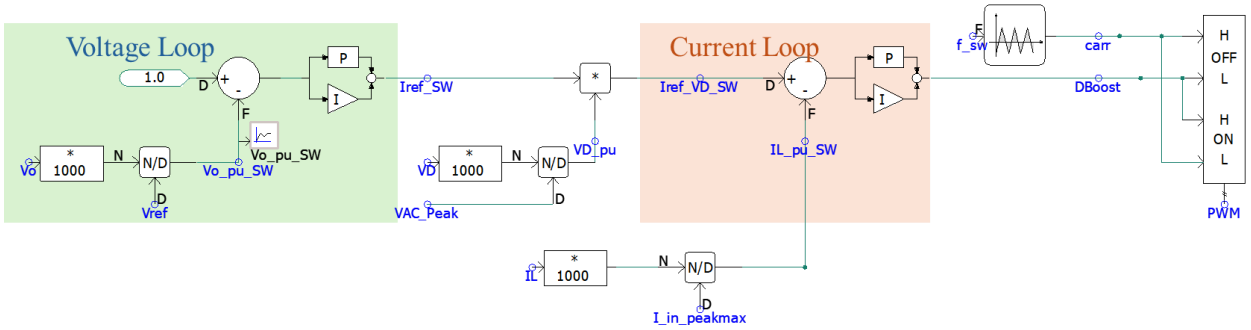

Figure 19: Dual-loop PI control for PFC circuit.

After obtaining the average reference inductor current, the transient current must be controlled to follow a rectified sine wave in phase with the rectified AC voltage V_D. To achieve this, the rectified voltage is multiplied by the average reference current I_{ref_SW} to generate the reference transient current $I_{ref\_VD\_SW}$. The rectified voltage V_D is converted to a per-unit value by dividing by the basic AC peak voltage, which is set as the nominal AC voltage $240\text{V} \times \sqrt{2}$. In this way, the phase information of the input voltage is extracted from V_{D_pu} as shown in Figure 20. Here, V_{D_pu} is a rectified sine wave with magnitude 1,

providing the voltage phase information. This signal is then used to control the instantaneous inductor current to be in phase with the voltage, effectively serving the same role as a phase-locked loop.

The reference current is achieved by controlling the IGBT's on and off duty. To this end, a current loop is employed to regulate the IGBT switching. The reference transient current is compared with the measured inductor current I_L. The measured current I_L is converted to per-unit value I_{L_pu} by dividing by the peak value, which is calculated based on the rated current, and I_{L_pu} thus ranges between 0 and 1. For further details on the PFC circuit, refer to [1].

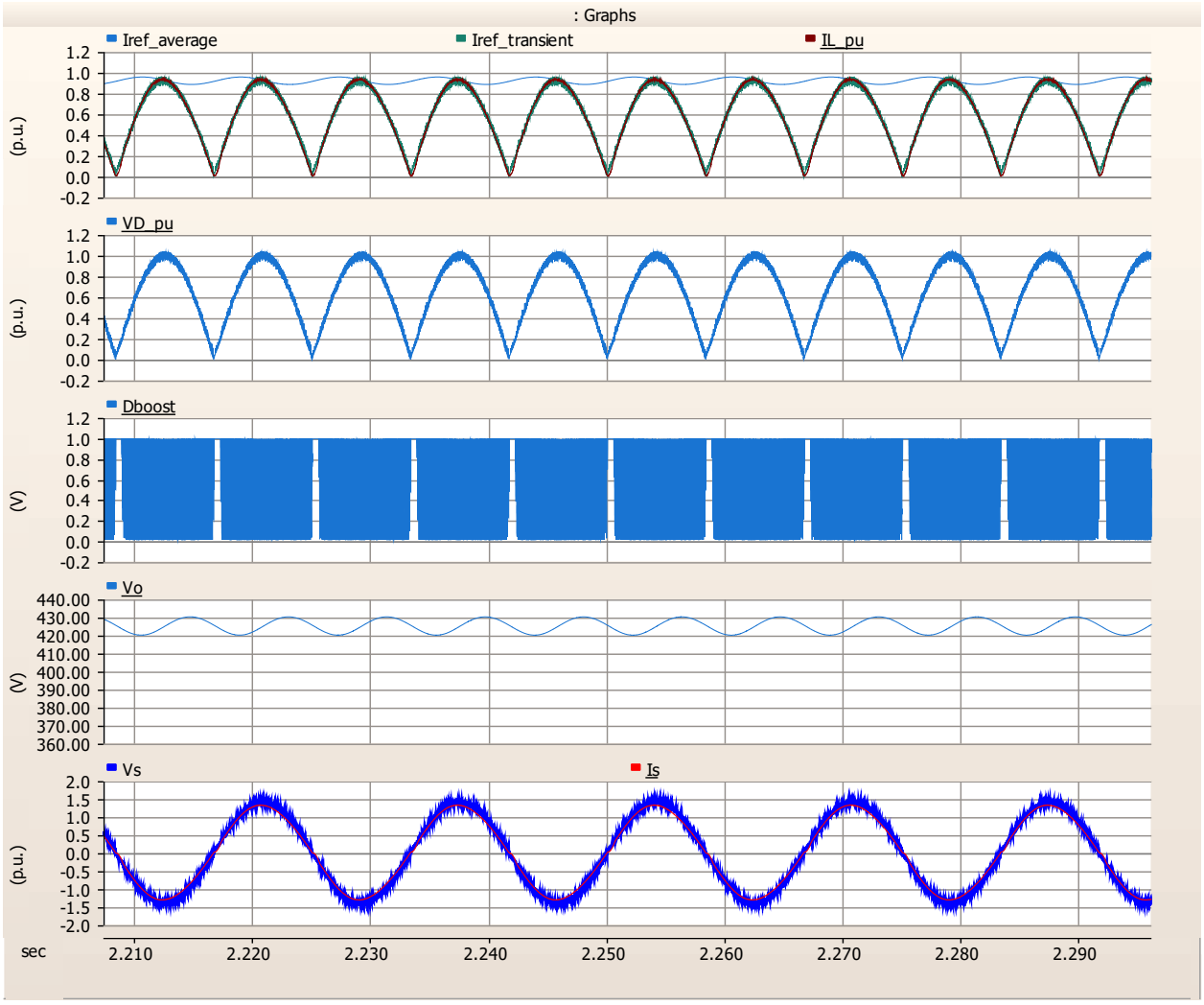

Figure 20: Inner signal of the dual-loop, the output DC voltage, and input AC voltage and current in steady state.

In the average model of the PFC, as shown in Figure 21, the switching IGBT is replaced by a controlled voltage source in series with the inductor and a controlled current source in parallel with the capacitor. The voltage source is controlled by $(1-D)V_{\mathrm{o}}$ and the current source is controlled by $(1-D)I_{\mathrm{L}}$, where D is the duty output from the dual-loop controller. For more details on the average model, refer to [1].

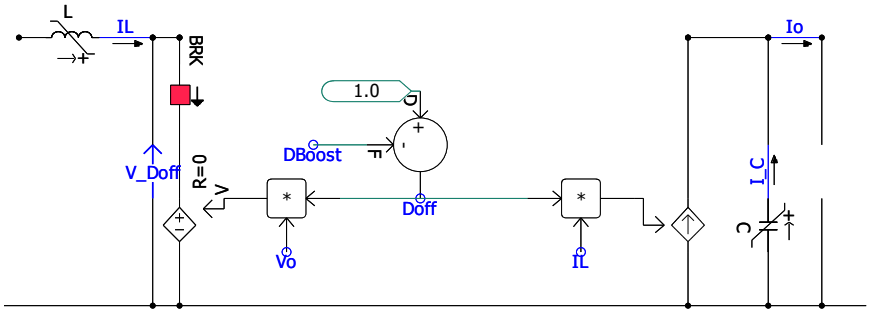

Figure 21: Average model of PFC circuit.

3.3. PI Controller Tuning and Voltage Ride-Through

3.3.1. Role of PI Controllers in VRT

When a **voltage sag** occurs on the AC side:

1) The outer voltage PI detects that the DC bus has dropped below 400 V.
2) It commands the inner current loop to increase the current intake.
3) The inner PI drives the boost converter switch, shaping the transient current to follow the phase of the AC voltage while increasing its magnitude according to the output of the outer voltage loop.

For a constant power load like the crypto miner, the control loops must be carefully tuned to manage this inherently negative-impedance behavior; otherwise, the system may oscillate or trip.

3.3.2. Effects of Proportional and Integral Gains of Outer Loop

1) Voltage dip response time
   - **Higher** K_{P}: faster correction of DC bus dips.

- **Higher** K_I: stronger integral action to eliminate steady-state errors, but excessive values can cause overshoots.
- **Excessively High** $\frac{K_P}{K_I}$: potential oscillations or overcurrent surges as the system attempts to restore voltage too aggressively.

2) System Oscillations and Damping
   - Fast, high-gain loops are prone to underdamped behavior, causing ringing in the DC voltage or input current.
   - Lower gains or carefully placed poles/zeros improved damping and a more stable ride-through, though recovery is slower.

3) Power Draw Fluctuations
   - During a sag, an aggressive PI controller can cause the miner to draw very high current, potentially worsening the sag for other loads or tripping its own protection.
   - A conservative PI may allow the DC bus voltage to sag more (reducing power draw) to preserve stability, but gains that are too low risk under-voltage.

4) Recovery Performance
   - **High gains**: rapid restoration of bus voltage after the sag but may cause overshoot (spike in DC voltage/current).
   - **Lower gains**: smoother, but slower, return to nominal voltage.

3.3.3. Trade-offs in PI Tuning for Large Flexible Loads

A critical trade-off exists between fast recovery (beneficial for miner uptime) and system stability (avoiding current or voltage overshoot). Tuning typically involves:

- **Bandwidth Separation**: A high-bandwidth inner current loop (~1–5 kHz) combined with a slower outer voltage loop (~5–20 Hz).
- **Moderate Phase Margin**: The voltage loop is often tuned with a generous margin (e.g., 60–80°) to handle the negative impedance effect of a constant power load.
- **Avoiding Saturation**: Clamping or limiting the PI output prevents integrator windup and control saturation during deep sags.

The voltage ride-through capability of a large, flexible load like the crypto miner strongly depends on PI controller tuning in its PFC stage. Properly selected proportional and integral gains enable the miner to:

- Respond swiftly to AC voltage dips,
- Maintain the DC bus above its undervoltage threshold,
- Avoid damaging current surges or oscillations upon recovery.

4. Model Benchmarking

To validate the developed PSCAD model, its low-voltage ride-through performance was benchmarked against laboratory measurements from a real crypto-miner. The model was parameterized based on a commercially available 3.5 kW crypto-miner. The device operates with a 240 V (RMS) AC input and a nominal DC-link voltage of 425 V. Additional specifications of the test device are summarized in Table 2. The test device is shown in Figure 22.

Table 2: Datasheet of the crypto-miner.

Crypto Algorithm	SHA-256
Optimal Power Efficiency (Joules/TH)	16[1]
Hashing Performance (TH/s at Joules/TH)	0-260 / xx Joules/TH at xxx TH/s[1]
Operating Temperature Range	-4 to 122°F (-20 to 50°C[2])
Power Supply	5000 Watts[3], 2 x C20 Input
Power Cables Included	2 x C19 to C20
Cooling Mechanism	Air-cooled
Power Supply AC Input Voltage, Nominal, Min/Max	200-240V, 180 - 264V
Power Supply AC Input Frequency	48-62 Hz
Power Supply AC Input Current	0-17.6 Amp per input

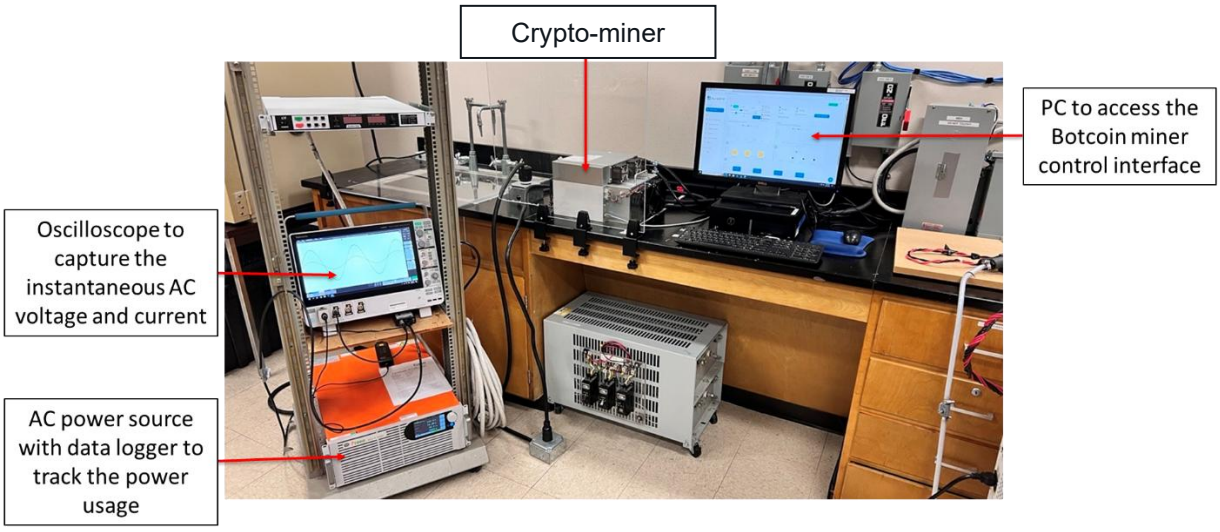

Figure 22: Real lab Test of the crypto-miner.

To verify the developed PSCAD model, two voltage sag scenarios are simulated to demonstrate that the transient dynamics closely match the real lab test results. The method for generating the faults is illustrated in Figure 23.

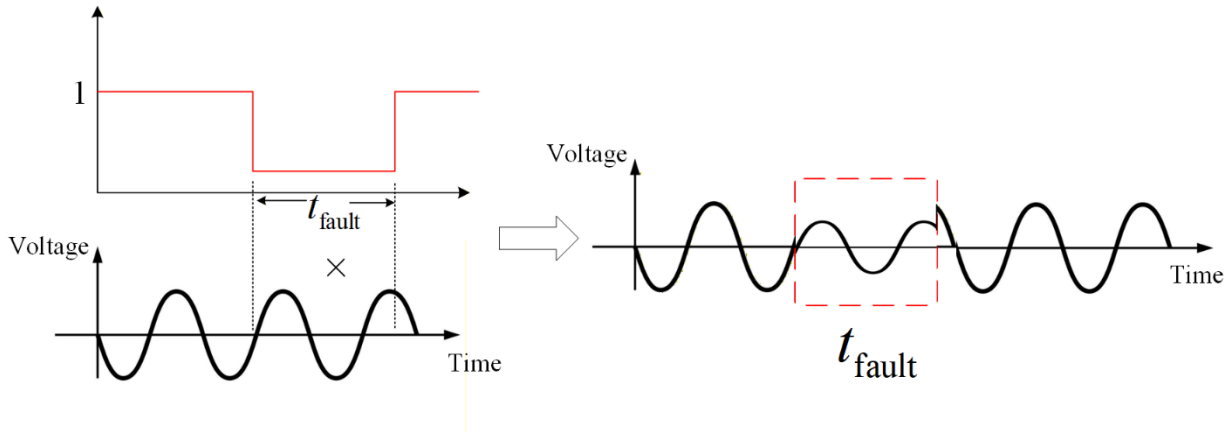

Figure 23: Fault setting method.

In PSCAD, the test case is constructed as shown in Figure 24, with the rated power set to 3.5 kW. Additional parameters are provided in Figure 25.

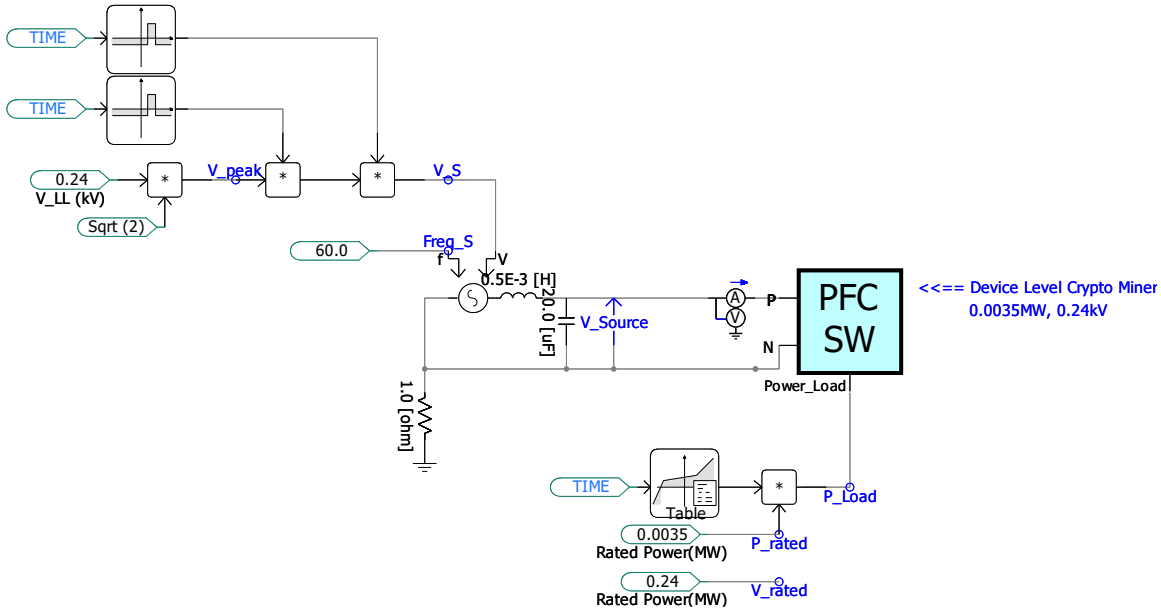

Figure 24: PSCAD case for model validation.

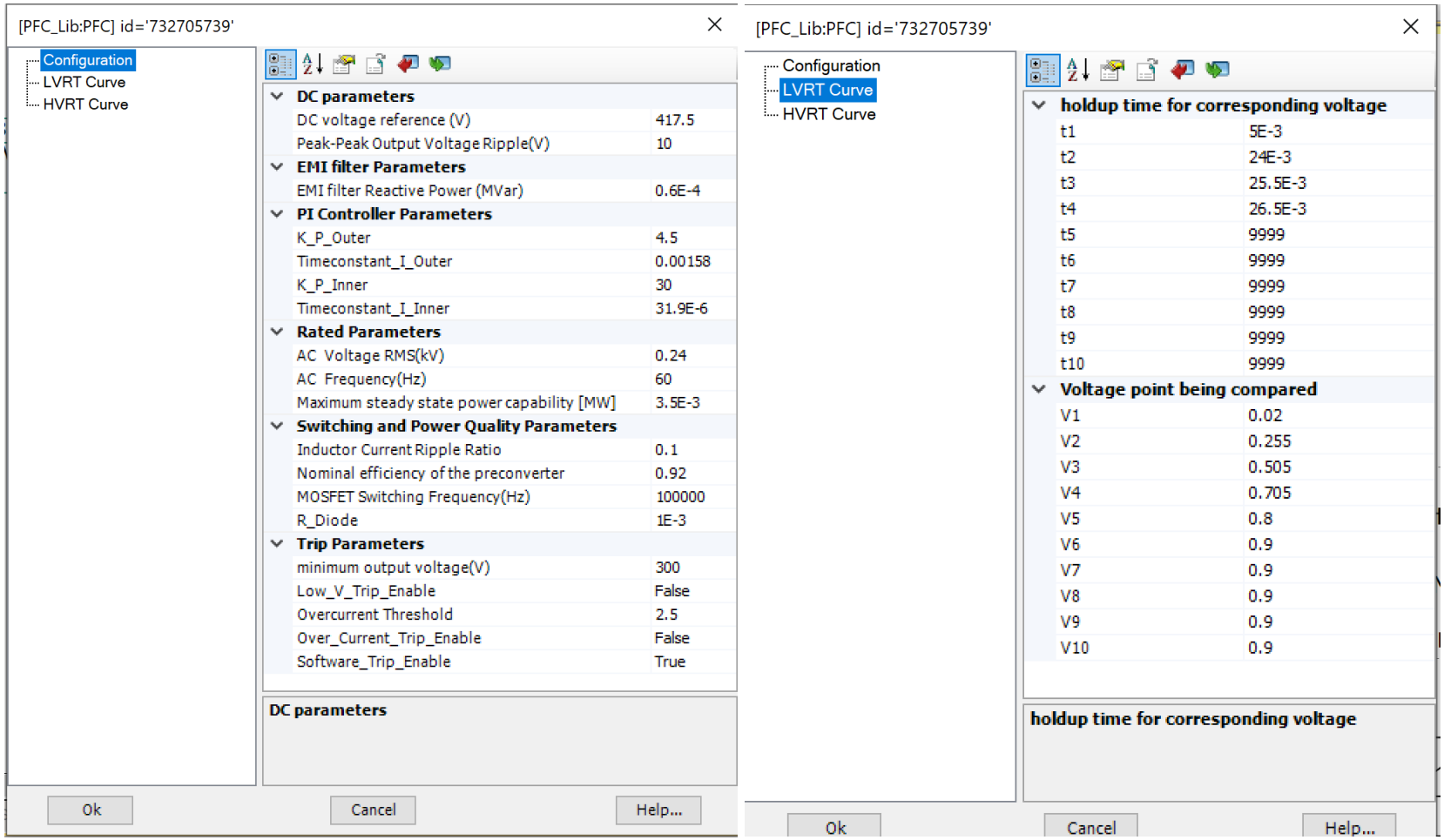

Figure 25: PSCAD parameters for model validation.

4.1. 168V (70%) Sag for 2 cycles (Trip)

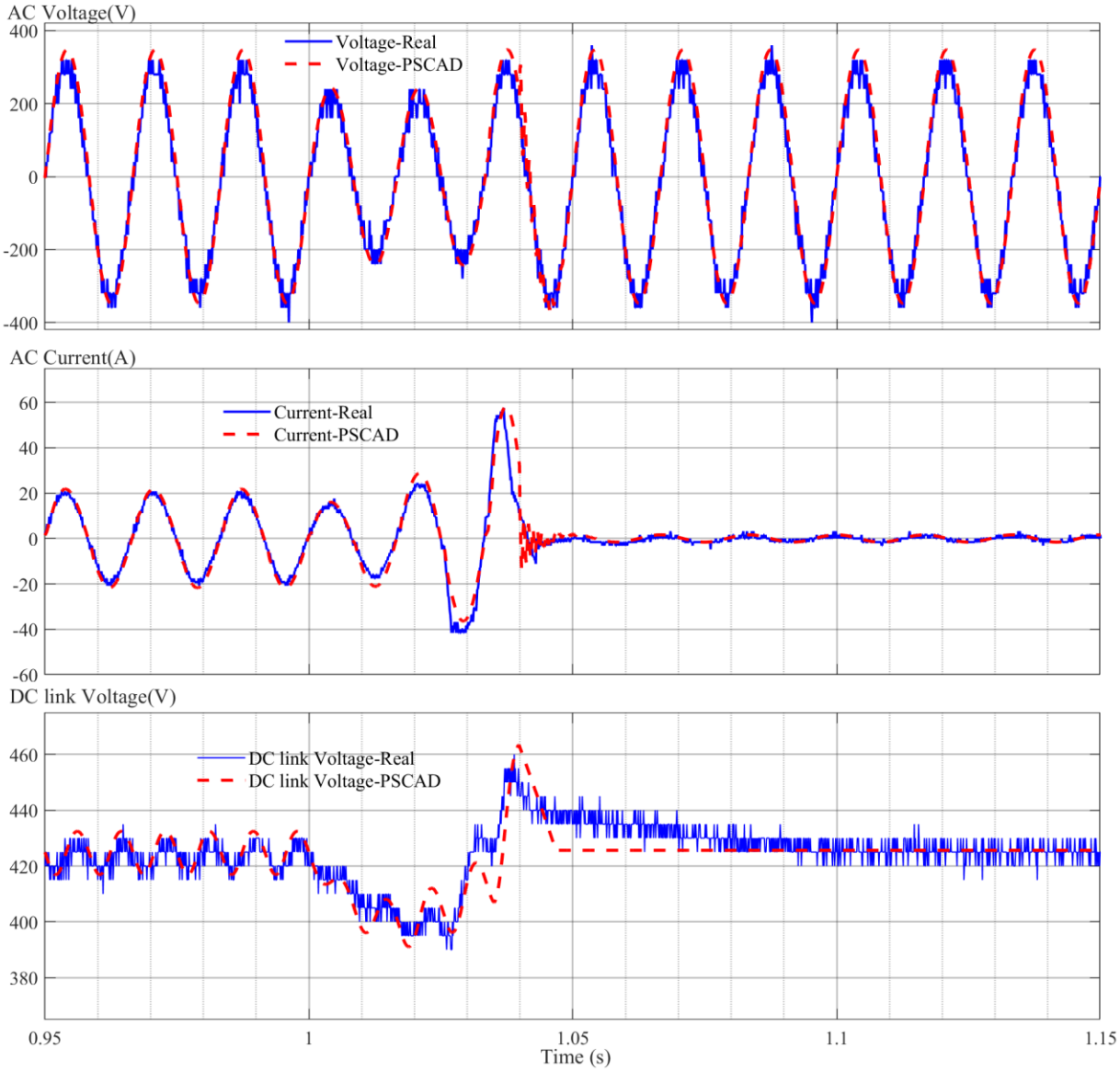

Figure 26: Voltage sags to 70% for 2 cycles. (Blue solid curves are real lab test results, and red dotted curves are PSCAD results).

Figure 26 compares the laboratory measurements and PSCAD simulation results for a 70% voltage sag lasting two cycles. During the voltage sag, the miner attempts to maintain the DC-side power by drawing additional input current, resulting in a significant increase in AC current magnitude. The reduced input voltage also causes a temporary drop in the DC-link voltage. When the voltage disturbance exceeds the ride-through capability of the miner, the protection mechanism is activated and the device trips,

causing the AC current to collapse to zero. The PSCAD model accurately reproduces the measured AC voltage, AC current, and DC-link voltage responses, including the transient current surge, DC-link voltage dynamics, and trip behavior. The close agreement between the simulation and laboratory results demonstrates the validity of the developed model for representing the LVRT performance of the crypto-miner.

4.2. 175V (73%) Sag (continuous operation)

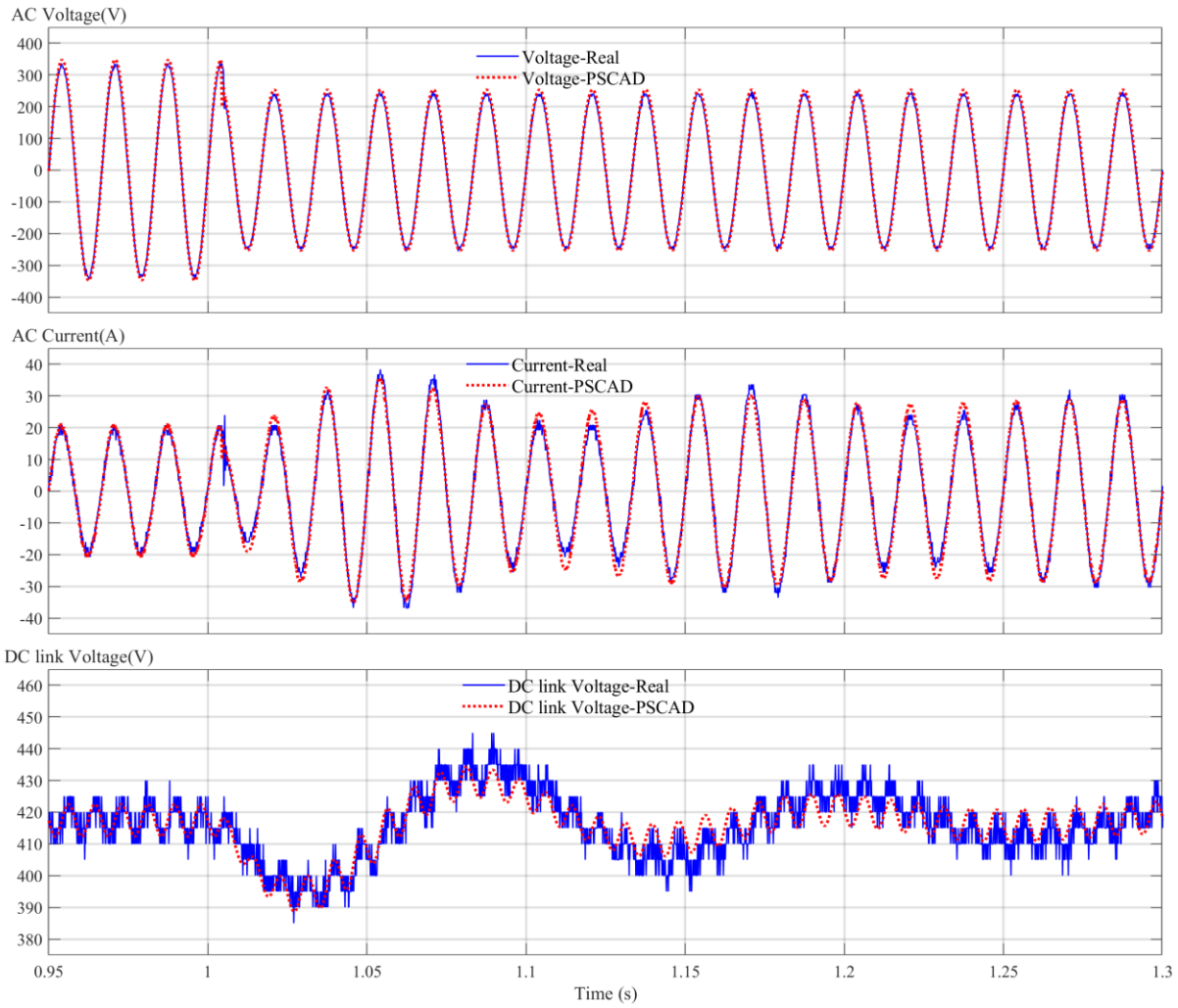

Figure 27: Voltage sags to 73% for 300ms (continuous operation) (Blue solid curves are real lab test results and red dotted curves are PSCAD results).

Figure 27 compares the laboratory measurements and PSCAD simulation results for a 73% voltage sag lasting 300 ms. Unlike the previous case, the miner remains in operation throughout the disturbance without triggering the protection mechanism. During the

voltage sag, the input current increases to maintain the required power demand, while the DC-link voltage experiences a temporary reduction followed by recovery after the voltage returns to its nominal value. The PSCAD model closely reproduces the measured AC voltage, AC current, and DC-link voltage responses, demonstrating its ability to accurately capture the continuous operating behavior of the crypto-miner during voltage disturbances within its ride-through capability.

5. Small-Signal Impedance Test Using Frequency Scanning

In this section, the input impedance of the developed model is tested based on the frequency scanning method.

5.1. Input Impedance Test Method

In this subsection, we examine the small-signal frequency response of the PSCAD model, as shown in Figure 28. The input impedance is measured by injecting a small-signal disturbance voltage of magnitude V_d at frequency f, and observing the resulting current magnitude I_d at that frequency. The small signal impedance at the frequency f is calculated as:

$$Z_f = \frac{V_d}{I_d}. \tag{5.1}$$

For the theoretical derivation, see [5].

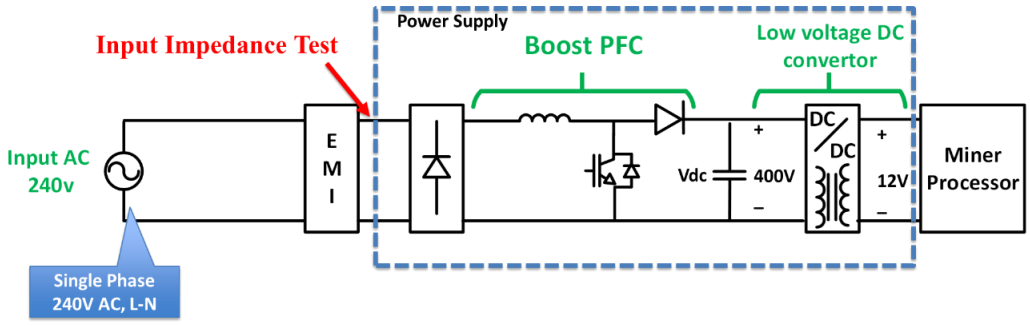

Figure 28: Input impedance test.

Both the average model and the switching model are tested in PSCAD using the method illustrated in Figure 29. A small-signal voltage of 2 V is injected. The load consists of a 3.3 kW resistor (48 ohm) corresponding to an equivalent AC-side resistance of 17.28 ohm. The input current is measured, and FFT analysis is performed to extract the current component at the same frequency as the injected disturbance. The disturbance frequency is swept from 5 to 50 Hz in 1 Hz steps. Each test runs for 3 s, and the steady-state current magnitude and phase at each frequency are recorded. The input impedance is then calculated according to (5.1).

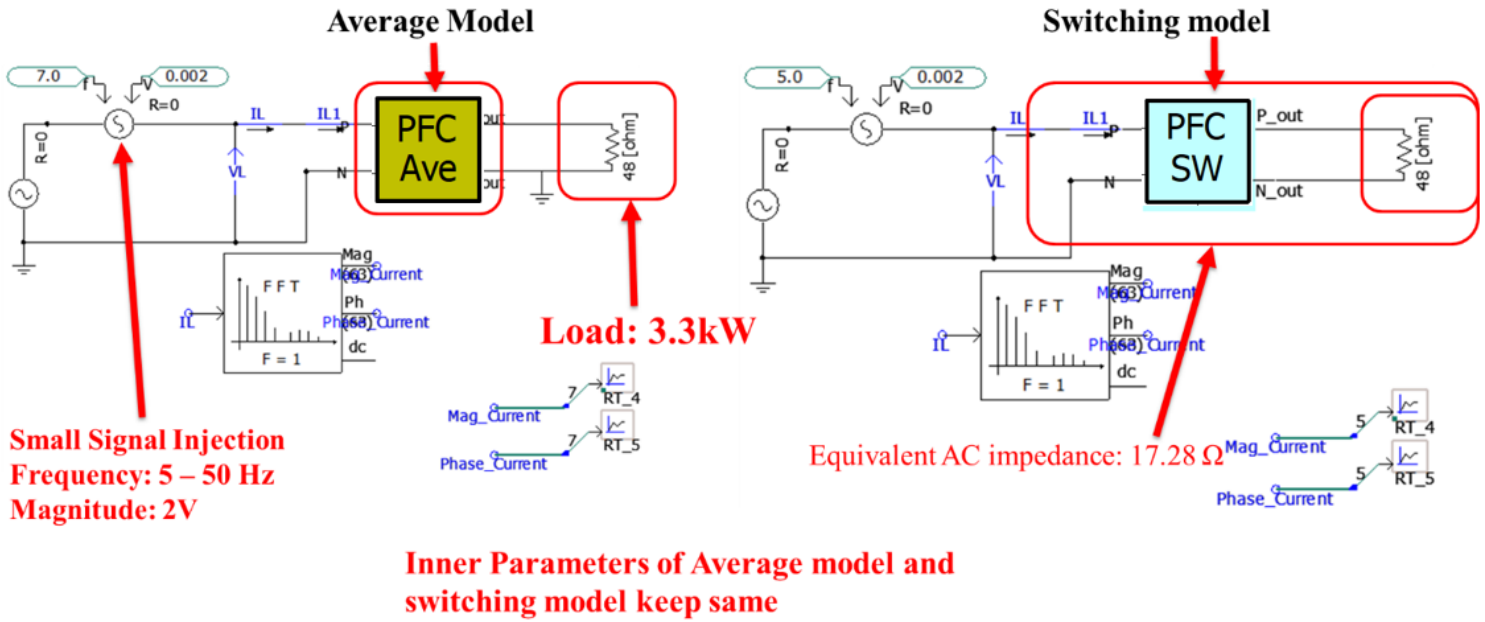

Figure 29: Input impedance test method.

5.2. Input Impedance Test Result

The input impedance test results for the average and switching models over the frequency range of 0–50 Hz are shown in Figure 30 and Figure 31, respectively. As expected, the input impedance characteristics of the average model closely match those of the switching model within this frequency range, demonstrating that the average model accurately captures the low-frequency dynamics of the switching model.

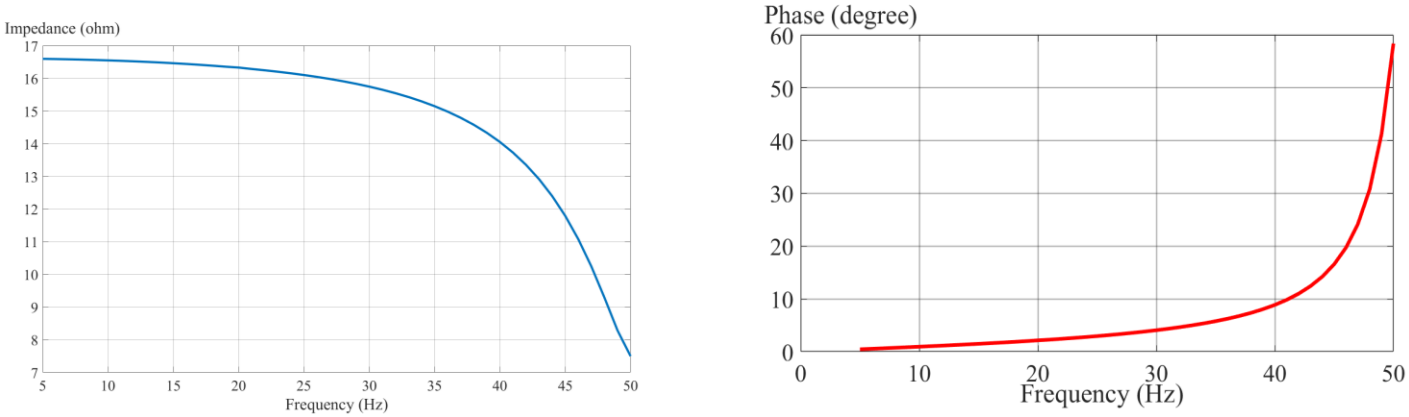

Figure 30: Input impedance test result of the average model.

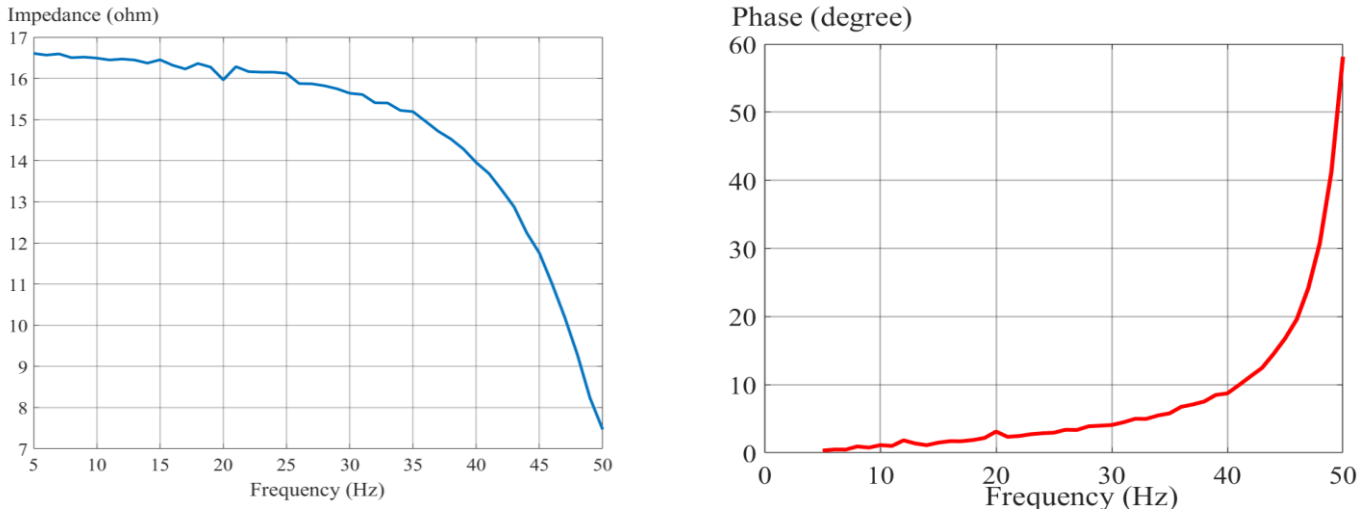

Figure 31: Input impedance test result of the switching model.

The input impedance of the switching model is further evaluated over the frequency range of 5 Hz to 2000 Hz, with the results shown in Figure 32. Two resonance points are identified at approximately 50 Hz and 70 Hz, which are consistent

with the results reported in [5] as illustrated in Figure 33. Detailed explanations of the mechanisms and locations of these resonance points can be found in the small-signal impedance models presented in [5] and [6].

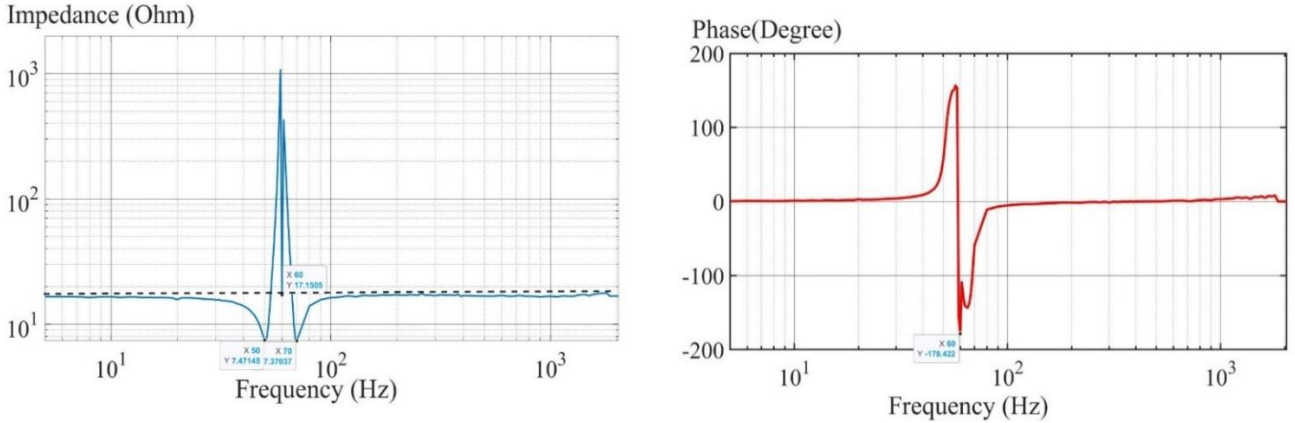

Figure 32: Input impedance test result of switch model (5Hz to 2000Hz).

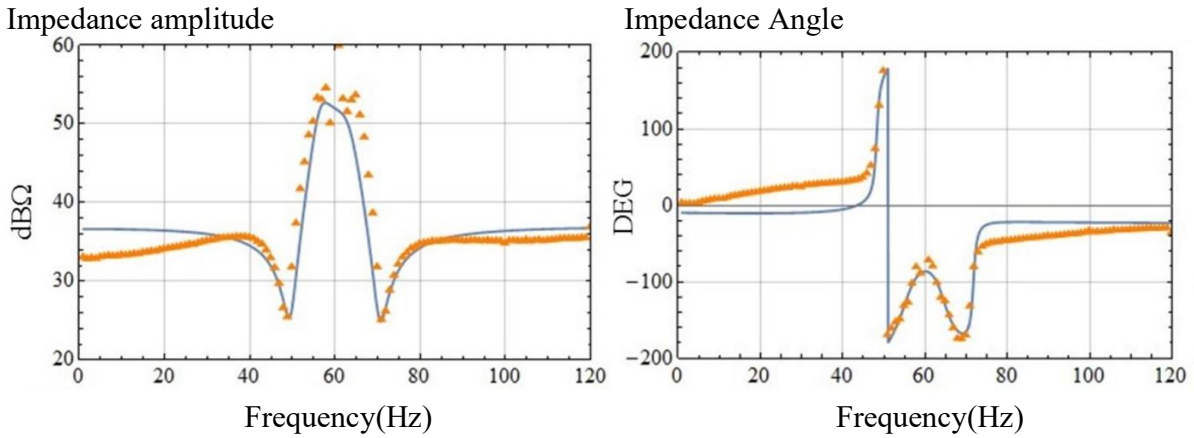

Figure 33： Input impedance of PFC in [5].

6. Device-Level and Facility-Level Test Case

In this section, the developed switching and average models of the crypto-miner load are evaluated in PSCAD through both device-level and facility-level case studies. At the device level, a 3.5 kW crypto-miner is connected to a 240 V AC source, and both load variations and grid voltage disturbances are applied to assess the dynamic performance of the two models. At the facility level, a 1 MW crypto-miner load is modeled for each phase, resulting in a total three-phase load of 3 MW. The load is subsequently scaled to represent a 300 MW crypto-mining facility connected to a 138 kV transmission system through two transformers. The dynamic responses of the switching and average models are recorded and compared under various operating conditions to evaluate their accuracy and consistency.

6.1. Device-Level Test Case

6.1.1. Test Electrical Circuit

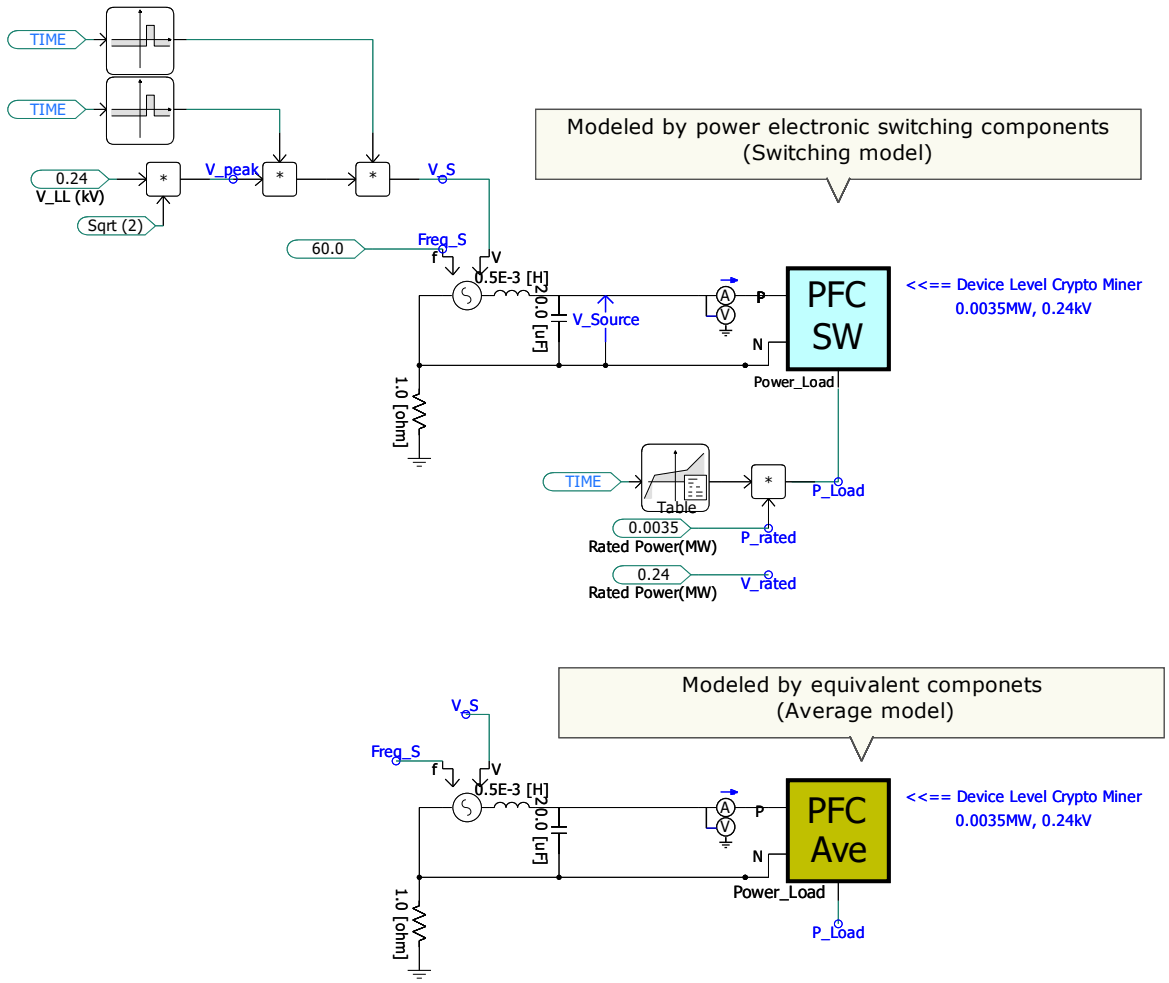

Figure 34: Device-level test case.

This case is included in the file **"CryptoMiner_Ave_SW_models.pscx"**. The electrical circuits are shown in Figure 34. Both the switching and average models are configured with a capacity of 3.5 kW and a rated AC voltage of 240 V. At 1.5 s, the AC voltage drops to 75% for 0.5 s and recovers at 2.0 s. At 2.5 s, the voltage drops to 55% for 24 ms and recovers at 2.524 s. At 3 s, the load decreases from 1 p.u. (3.5 kW) to 0.5 p.u. (1.75 kW) over 0.1 s.

The parameter settings of the switching and average models are configured as shown in Figure 35.

DC parameters	
DC voltage reference (V)	417.5
Peak-Peak Output Voltage Ripple(V)	10
EMI filter Parameters	
EMI filter Reactive Power (MVar)	0.00016
PI Controller Parameters	
K_P_Outer	4.5
Timeconstant_I_Outer	0.00158
K_P_Inner	30
Timeconstant_I_Inner	31.9E-6
Rated Parameters	
Maximum steady state power capability [MW]	P_rated
AC Voltage RMS(kV)	V_rated
AC Frequency(Hz)	60
Switching and Power Quality Parameters	
Inductor Current Ripple Ratio	0.1
Nominal efficiency of the preconverter	0.92
MOSFET Switching Frequency(Hz)	10000
R_Diode	1E-3
Trip Parameters	
minimum output voltage(V)	300
Overcurrent Threshold	2.5
Over Voltage Trip enabled (=1) disabled (=0)	0
Over Current Trip enabled (=1) disabled (=0)	0
VRT Curve enabled (=1) disabled (=0)	1
Time delay to activate the trip settings(s)	0.2

(a) Switching Model

DC parameters	
DC voltage reference (V)	417.5
Peak-Peak Output Voltage Rippl	10
EMI filter Parameters	
EMI filter reactive power (MVar)	0.00016
PI Controller Parameters	
K_P_Outer	4.5
Timeconstant_I_Outer	0.00158
K_P_Inner	30
Timeconstant_I_Inner	31.9e-6
Rated Parameters	
Maximum steady state power ca	P_rated
AC Voltage RMS(kV)	V_rated
AC Frequency(Hz)	60
Switching and Power Quality Parameters	
Inductor Current Ripple	0.1
MOSFET Switching Frequency(H:	10000
Nominal efficiency of the precor	0.92
R_Diode	5e-3
Trip Parameters	
minimum output voltage(V)	300
OverCurrentThreshold (pu)	2.5
Over Voltage Trip enabled (=1)	0
Over Current Trip enabled (=1)	0
VRT Curve enabled (=1) disable	1
Time delay to activate the trip s	0.2

(b) Average Model

Figure 35: Parameters configuration for the test case.

P_rated is set to 0.0035 MW, and V_rated is set to 0.24 kV. Since the EMI filter is predominantly capacitive, it is represented by an equivalent capacitor in the model. The reactive power of the equivalent capacitor is set to 160 var.

6.1.2. Test Result

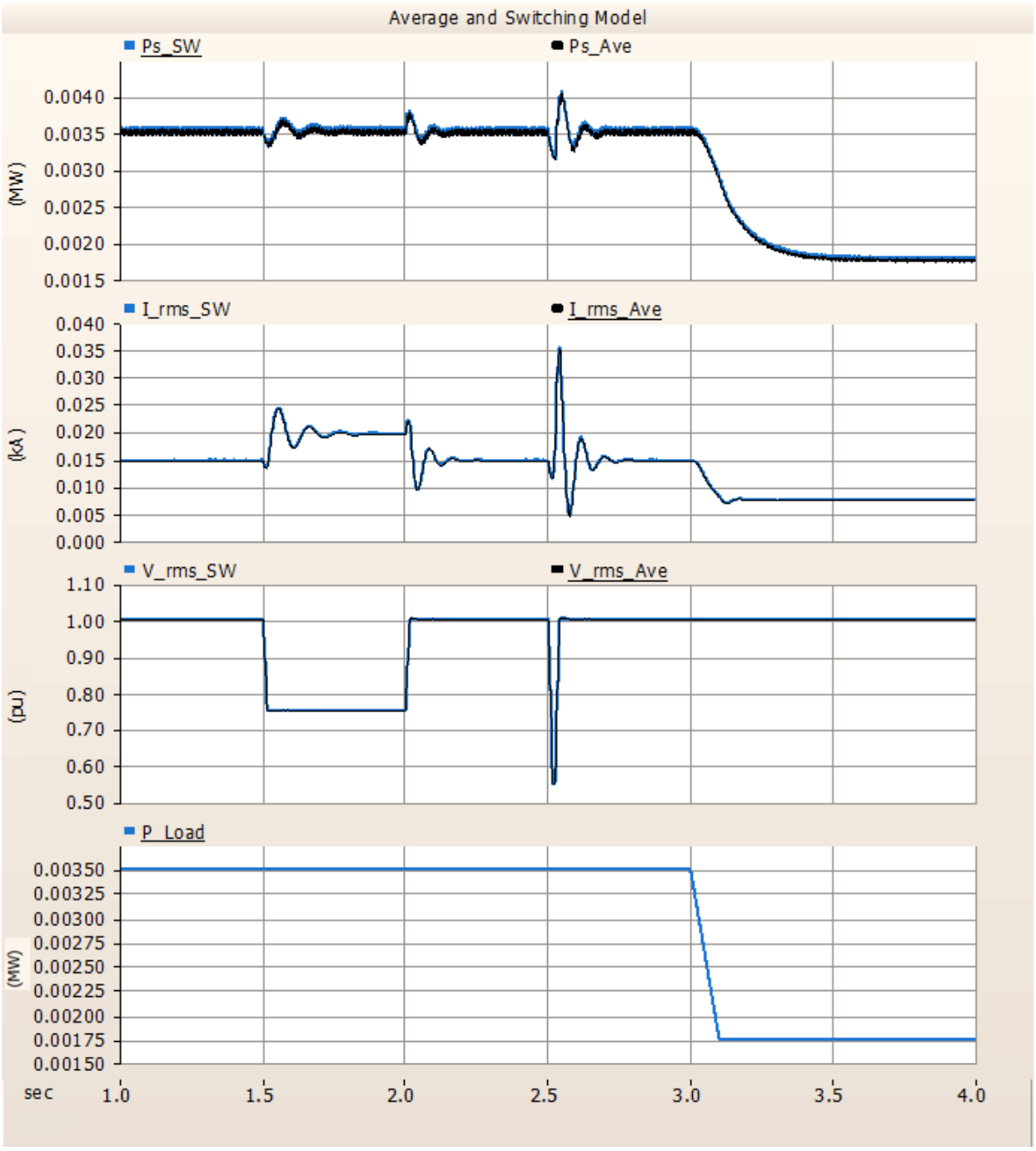

Figure 36: Device level test result: AC power (Ps_SW for switching model and Ps_Ave for average model), Current (RMS value, I_rms_SW for switching model and I_rms_Ave for average model), Voltage (RMS value, V_rms_SW for switching model and V_rms_Ave for average model), and Computing Load (DC side constant power load P_Load).

The grid-side responses are shown in Figure 36, demonstrating good agreement between the switching and average models. In both models, the measured AC-side power is

slightly higher than the specified DC-side constant power load. This difference is attributed to power losses in the diodes, IGBT, and the resistors connected in parallel with the DC-link capacitor.

The DC-link voltage responses of the switching and average models are shown in Figure 37. The results exhibit close agreement, further confirming the accuracy of the average model in reproducing the dynamic behavior of the switching model.

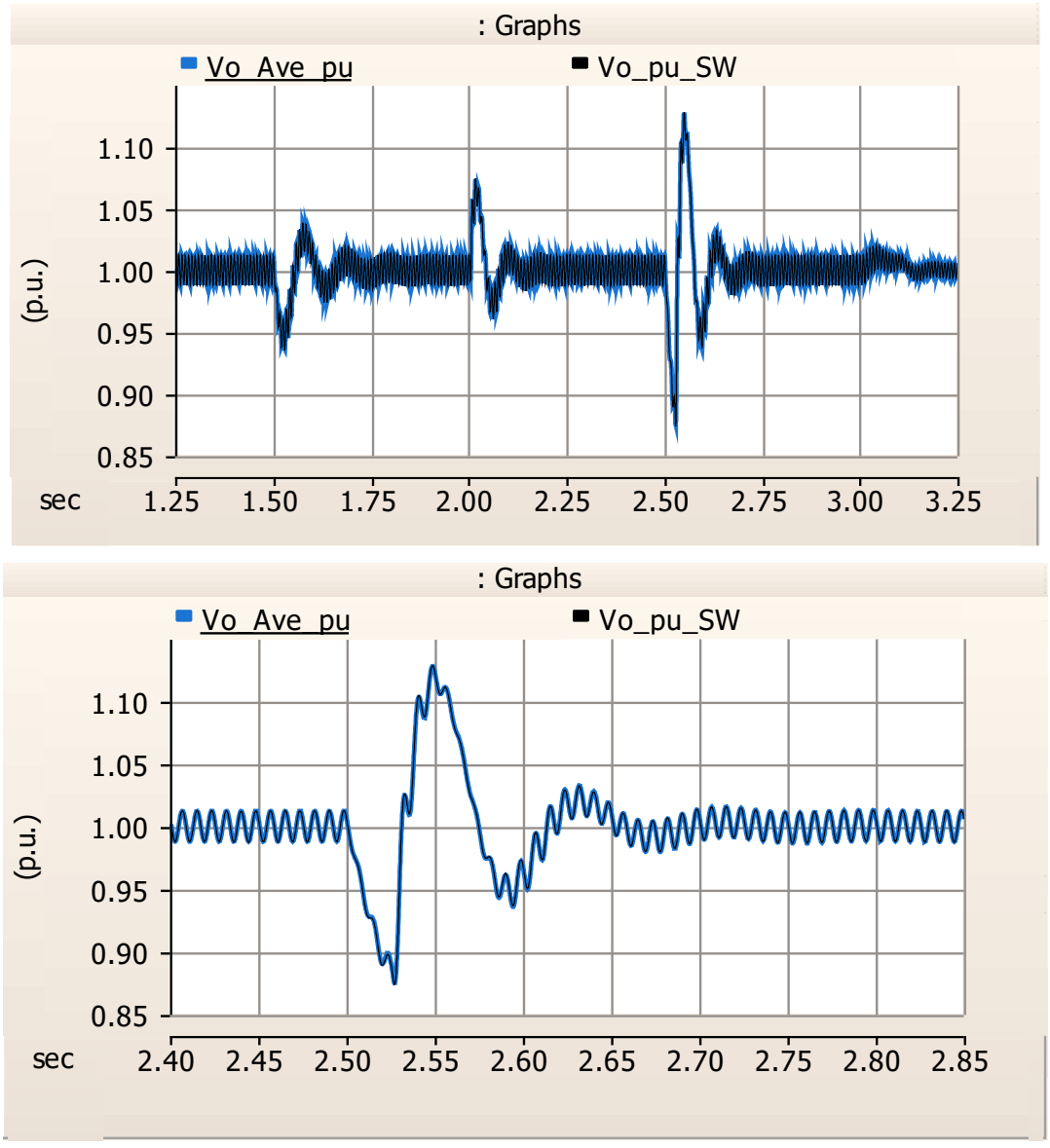

Figure 37: DC link voltage of the switching model and the average model. (Vo is the DC link voltage in per unit value, and the base value is 400 V. The figure below is a zoomed-in view of the figure above.)

6.2. Facility Level Test Case

6.2.1. Test Electrical Circuit

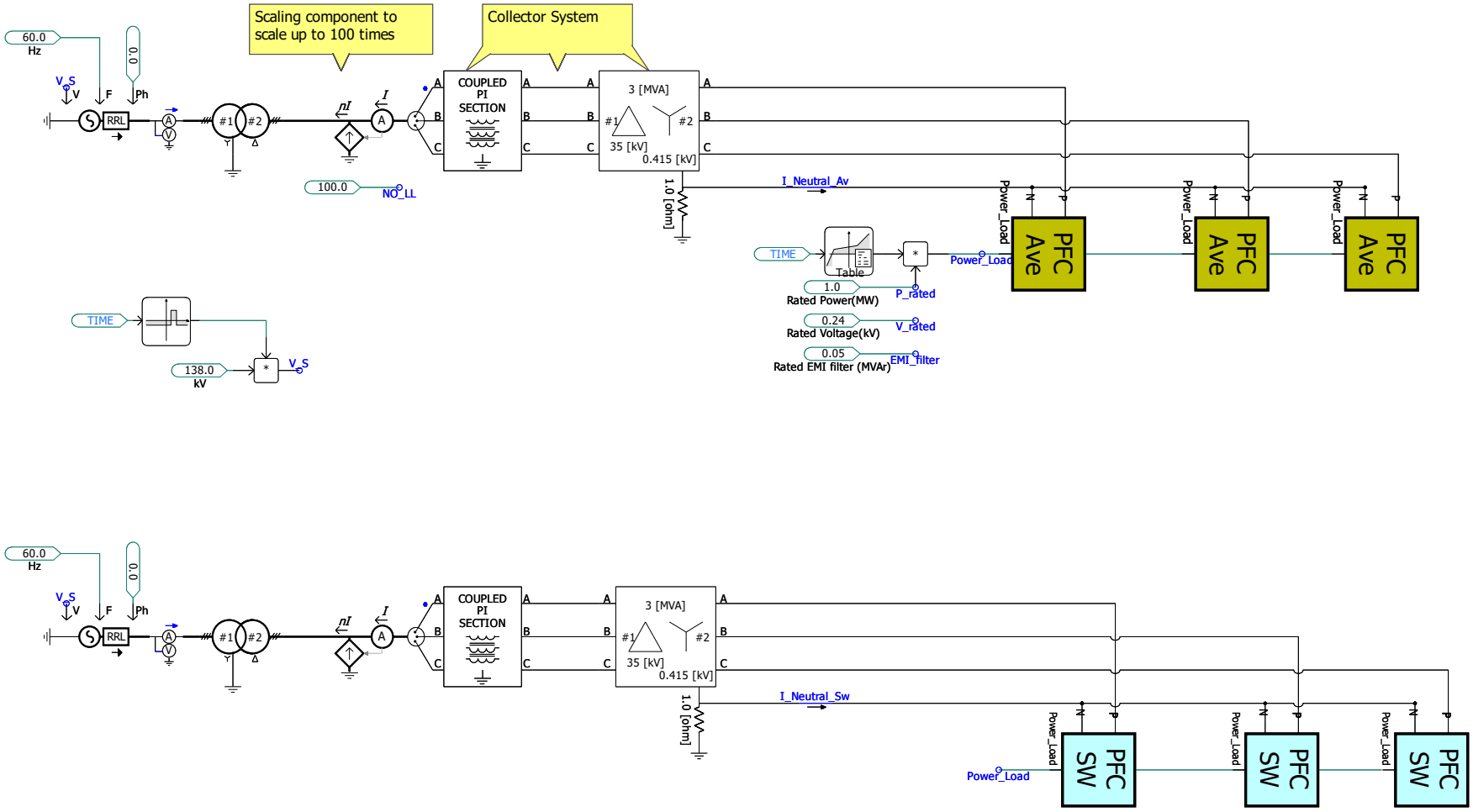

Figure 38: Facility Level Test case.

This case is included in the file **"**CryptoMiner_SW_Ave_Facility.pscx**".** In this case, the crypto-miner model is configured with a rated power of 1 MW per phase at 240 V, resulting in a total three-phase load of 3 MW. The load is connected to a collector system consisting of a 3 MVA, 35 kV/0.45 kV transformer and a π-section transmission line. To represent a large-scale crypto-mining facility, a scaling factor of 100 is applied, yielding an equivalent load of 300 MW. The scaled load is connected to the transmission system through a 300 MVA, 138 kV/35 kV transformer and is ultimately tied to the bulk power grid. The electrical configuration of the test system is shown in Figure 38.

6.2.2. Test Results

The load is initially ramped from 0 MW to 75 MW (0.75 p.u.) over 0.5 s, starting at $t = 0$ s. At $t = 3$ s, the load is further increased from 75 MW to 300 MW (3.0 p.u.) over 0.1 s. At $t = 5$ s, the voltage on the 138 kV side is reduced to 80% of its nominal value and remains at this level until $t = 5.5$ s, after which it recovers to its nominal value.

The voltage, active power, and reactive power responses are shown in Figure 39. The active power responses of the switching and average models are in close agreement throughout the simulation. A small difference is observed in the reactive power response due to the presence of 10 kHz switching harmonics in the switching model, which introduce additional reactive power losses in the transformers. When the grid voltage drops to 80% at $t = 5$ s, the current increases from 3.0 p.u. to approximately 3.75 p.u. to maintain constant power consumption. As a result, the transformer reactive power losses increase, leading to a corresponding rise in reactive power demand.

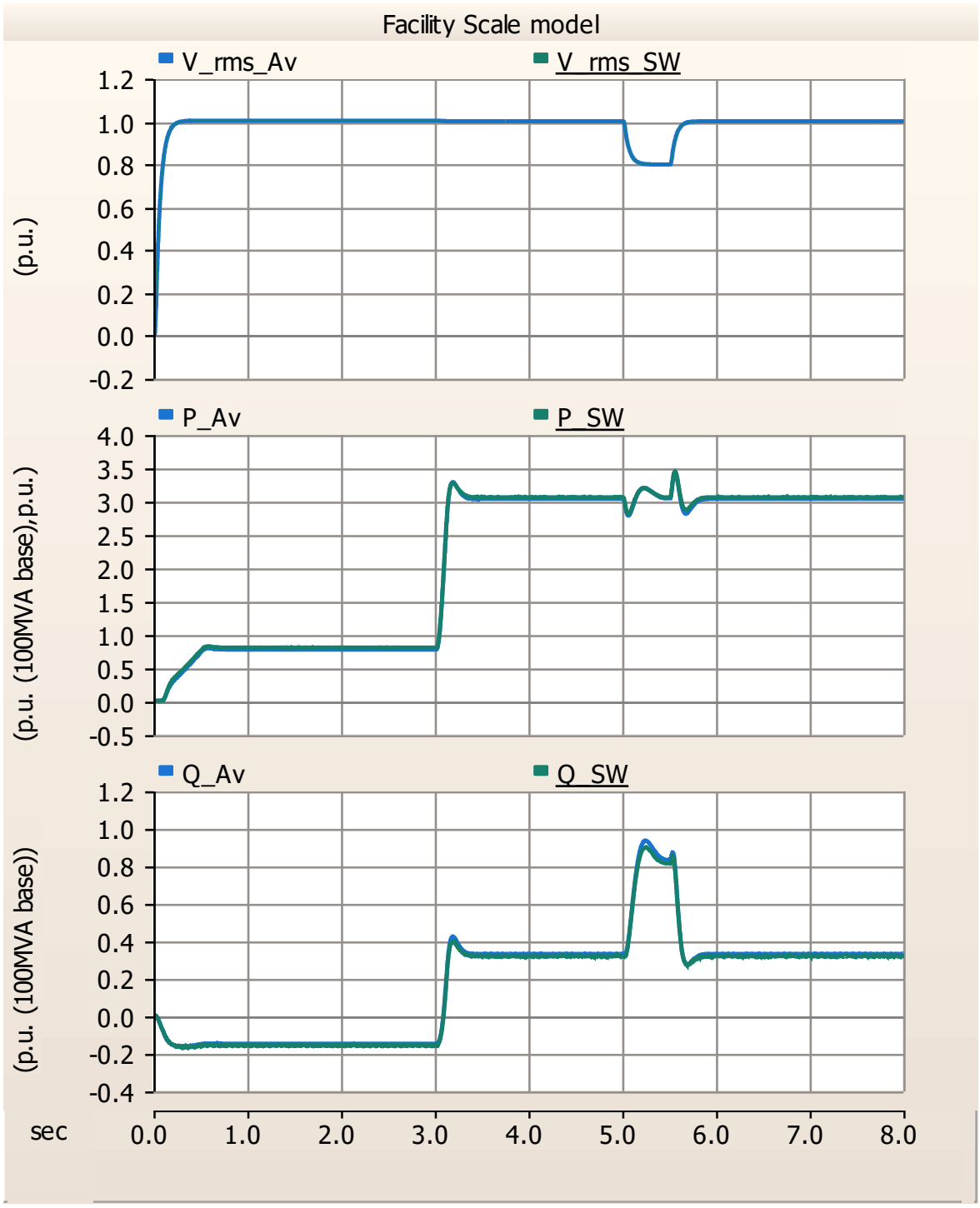

Figure 39: Facility Level Test Result. (P_Av and P_SW denote the active power measured on the 138 kV side for the average and switching models, respectively. Q_Av and Q_SW denote the corresponding reactive power on the 138 kV side. All power quantities are expressed on a 100 MVA base. V_rms_Av and V_rms_SW represent the RMS voltage measured on the 138 kV side for the average and switching models, respectively.)

7. Conclusion

This report developed and validated open-source PSCAD-based EMT models for crypto-miner loads to support transmission reliability and large flexible load studies. The proposed models capture the fundamental behavior of crypto-miners through a PFC-based front-end converter and constant power computing load representation. Both switching and average model implementations are provided, allowing users to select the appropriate balance between simulation accuracy and computational efficiency.

Benchmarking against laboratory test data demonstrated that the models accurately reproduce low-voltage ride-through performance, transient current response, DC-link voltage dynamics, and protection behavior during voltage disturbances. The developed VRT framework, including DC-link undervoltage protection, overcurrent protection, and user-configurable LVRT/HVRT curves, enables the models to capture both continuous operation and trip behavior under a wide range of grid voltage conditions. The close agreement between simulation and laboratory measurements confirms the capability of the models to accurately represent the dynamic response of real crypto-mining devices during voltage sag events.

Frequency-domain analysis further verified that the developed models capture the low-frequency impedance characteristics relevant to power system stability studies. Device-level and facility-level simulations showed strong agreement between the switching and average models, confirming the suitability of the average model for large-scale EMT simulations while maintaining sufficient accuracy.

Overall, the developed models provide a practical and validated framework for studying the impacts of large-scale crypto-mining facilities on power system dynamics, voltage stability, and voltage ride-through performance. The modeling approach can also serve as a foundation for future EMT representations of other power-electronics-interfaced large flexible loads, including AI data centers and advanced computing facilities.

8. References

[1] L. Bao, L. Fan and Z. Miao, "Modeling and Analysis of Single-phase Boost Converter with Power Factor Correction Control," 2020 52nd North American Power Symposium (NAPS), Tempe, AZ, USA, 2021, pp. 1-6.
[2] Information Technology Industry Council (ITIC), “ITI (CBEMA) Curve Application Note,” 2000.
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[4] Toshiba Electronic Devices & Storage Corporation. “Power Factor Correction (PFC) Circuits Application Note.” 2019. https://toshiba.semicon-storage.com/info/docget.jsp?did=68570
[5] J. Sun, M. Xu, M. Cespedes and M. Kauffman, "Low-Frequency Input Impedance Modeling of Single-Phase PFC Converters for Data Center Power System Stability Studies," 2019 IEEE Energy Conversion Congress and Exposition (ECCE), Baltimore, MD, USA, 2019, pp. 97-106
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