- P-E ERCOT presentation

- S. Giguere
- Director of Energy Storage U.S.
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Agenda

- Voltage Ride Through Table A
- TOV Table B
- Frequency Ride Through
- Phase Angle Jump
- PSSE and PSCAD models
- Backwards Compatibility
- Timeline

NOGR 245 Summary - Inverters

	Status	comment
▪ Voltage Ride Through Table A	Comply	Do not comply for legacy HEC units
▪ TOV Table B		Testing scheduled W14/W15
▪ Frequency Ride Through	Comply for all units	
▪ Phase Angle Jump	Comply for Gen. 3	Recommend matching IEEE-2800 requirements
▪ PSSE and PSCAD models	Existing model files will work.	No updates required
▪ Backwards Compatibility	Uncertain if inverters operating today require software or hardware retrofits	
▪ Timeline	Need IEEE-2800 test standards released	

P-E NOGRR -245 Compliance by Inverter Family

	Gen3	Gen2	Gen1	HEC-US	Comments
Voltage Ride Through Table A	Y	Y			
TOV Table B					Testing in Q2
Frequency Ride Through	Y	Y	Y		
Phase Angle Jump	Y				Reduced to 25 degrees
PSSE and PSCAD models	Y				
Comply without retrofits	Y		N	N	
Timeline					

DRAFT – updated table pending

Fast Frequency Response

- Individual Inverter Responses vs system responses

Appendix

NOGRR-245 Voltage Ride Through Table A

Proposed P-E Voltage Protection settings

Voltage Ride-Through Requirements for Transmission-Connected Inverter-Based Resources (IBRs)

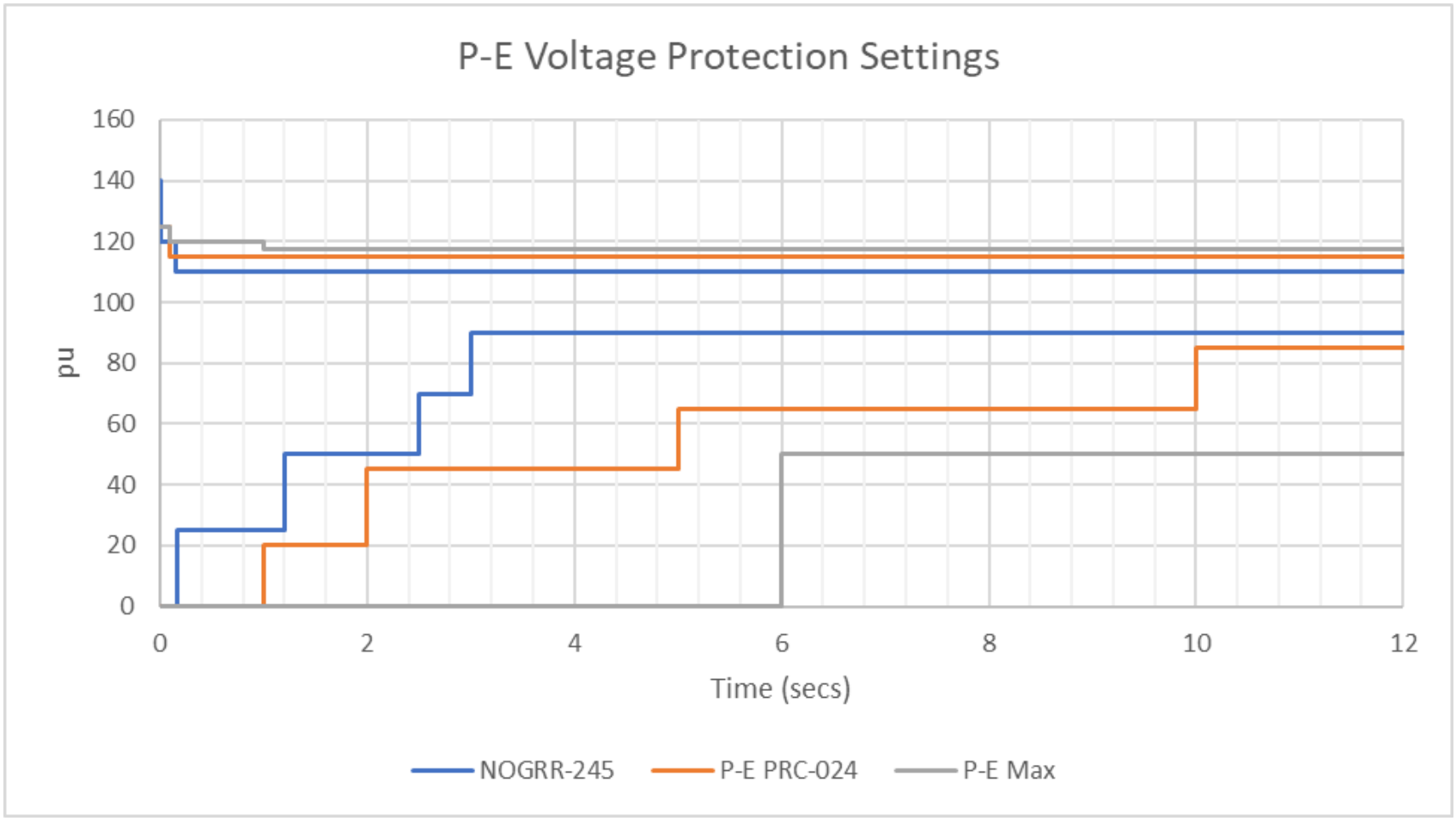
Table A

Root-Mean-Square Voltage (p.u. of nominal)	Minimum Ride-Through Time (seconds)
V > 1.20	No ride-through requirement
1.10 < V ≤ 1.20	1.0
0.90 ≤ V ≤ 1.10	continuous
0.70 ≤ V < 0.90	3.0
0.50 ≤ V < 0.70	2.5
0.25 ≤ V < 0.50	1.2
V < 0.25	0.16

Low Input Voltage			
G5.1.1	Low V Enable	YYYYN	-
G5.1.2	Slow Protection	85.0	%
G5.1.3	Delay for Slow Protection (0.0 – 6550.0)	10	sec
G5.1.4	Fast Protection	65	%
G5.1.5	Delay for Fast Protection (0.00-655.00)	5	sec
G5.1.6	Fast 2 Protection	45	%
G5.1.7	Delay for Fast 2 Protection (0.00-655.00)	2	sec
G5.1.8	Very Fast Protection	20	%
G5.1.9	Delay for Very Fast Protection (0.000-65.500)	1	sec
G5.1.10	Second Very Fast 2 Protection	Disabled	%
G5.1.11	Delay Very Fast 2 Protection (0.000-65.500)	Disabled	sec

High Input Voltage			
G5.2.1	High V Enable	YYNYN	-
G5.2.2	Slow Protection	115.0	%
G5.2.3	Delay for Slow Protection (0.0 – 6550.0)	2	sec
G5.2.4	Fast Protection	125	%
G5.2.5	Delay for Fast Protection (0.00-655.00)	0.1	sec
G5.2.6	Fast 2 Protection	Disabled	%
G5.2.7	Delay for Fast 2 Protection (0.00-655.00)	Disabled	sec
G5.2.8	Very Fast Protection	140.0	%
G5.2.9	Delay for Very Fast Protection (0.000-65.500)	0.003	sec
G5.2.10	Second Very Fast 2 Protection	Disabled	%
G5.2.11	Delay Very Fast 2 Protection (0.000-65.500)	Disabled	sec

P-E Voltage Protection settings for ERCOT Inverters



NOGRR-245 Voltage Ride Through Table B

Table B

Instantaneous Phase Voltage (p.u. of nominal)	Minimum Ride-Through Time (milliseconds)
V > 1.80	No ride-through requirement
1.70 < V ≤ 1.80	0.2
1.60 < V ≤ 1.70	1.0
1.40 < V ≤ 1.60	3.0
1.20 < V ≤ 1.40	15.0

Under study. Testing Scheduled for W14-W15

2.9.1 Multiple Voltage Excursions

- (7) The IBR shall ride through multiple excursions outside the continuous operation range in Table A in paragraph (1) above, unless the conditions and situations specified below exist, in which the IBR **may** trip to protect equipment from the cumulative effect of successive voltage deviations:
  - (a) More than four voltage deviations at the POIB outside the continuous operation zone within any ten second period.
  - (b) More than six voltage deviations at the POIB outside the continuous operation zone within any 120 second period.
  - (c) More than ten voltage deviations at the POIB outside the continuous operation zone within any 1,800 second period.
  - (d) Voltage deviations outside of continuous operation zone in Table A in paragraph (1) above following the end of a previous deviation by less than twenty cycles of system fundamental frequency.
  - (e) More than two individual voltage deviations at the POIB below 50% of the nominal voltage (including zero voltage) within any ten second period.
  - (f) More than three individual voltage deviations at the POIB below 50% of the nominal voltage (including zero voltage) within any 120 second period.

NOGRR-245 Frequency Ride Through

2.6.2 *Generators and Energy Storage Resources*

(1)

Frequency Range	Delay to Trip
Above 59.4 Hz	No automatic tripping (Continuous operation)
Above 58.4 Hz up to And including 59.4 Hz	Not less than 9 minutes
Above 58.0 Hz up to And including 58.4 Hz	Not less than 30 seconds
Above 57.5 Hz up to And including 58.0 Hz	Not less than 2 seconds
57.5 Hz or below	No time delay required

(2)

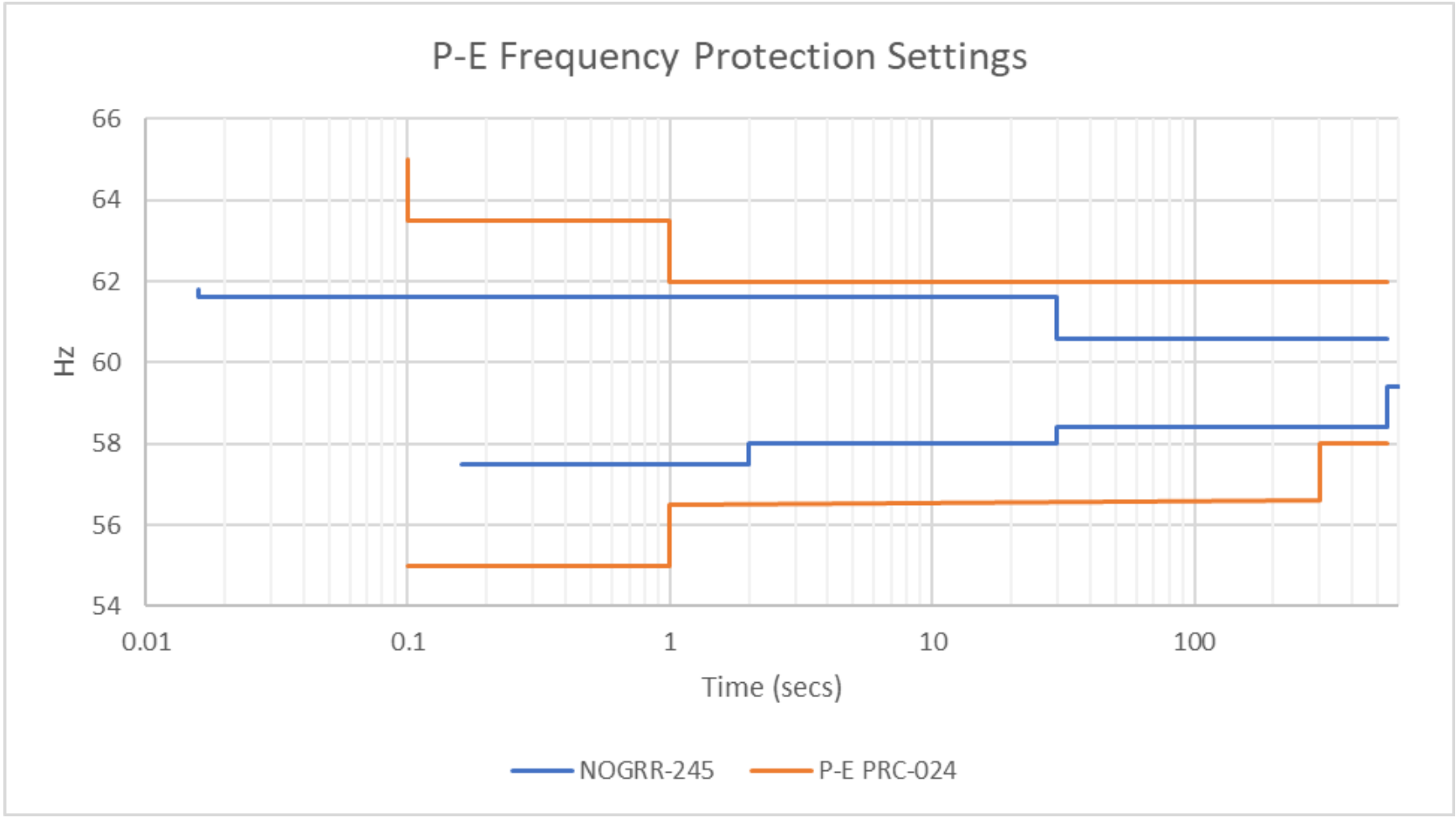
Frequency Range	Delay to Trip
Below 60.6 Hz down to and including 60 Hz	No automatic tripping (Continuous operation)
Below 61.6 Hz down to and including 60.6 Hz	Not less than 9 minutes
Below 61.8 Hz down to and including 61.6 Hz	Not less than 30 seconds
61.8 Hz or above	No time delay required

Proposed P-E Frequency Protection settings

Low Input Frequency			
G5.3.1	Low f Enable	YNYYN	-
G5.3.2	Slow Protection	58	Hz
G5.3.3	Delay for Slow Protection (0.0 – 6550.0)	300	Second
G5.3.4	Slow 2 Protection	Disabled	Hz
G5.3.5	Delay for Slow 2 Protection (0.0 – 6550.0)	Disabled	Second
G5.3.6	Fast Protection	56.5	Hz
G5.3.7	Delay for Fast Protection (0.00-655.00)	1.0	Second
G5.3.8	Very Fast Protection	55.0	Hz
G5.3.9	Delay for Very Fast Protection (0.000-65.500)	0.1	Second
G5.3.10	Very Fast 2 Protection	Disabled	Hz
G5.3.11	Delay for Very Fast 2 Protection (0.000-65.500)	Disabled	Second

High Input Frequency			
G5.4.1	High f Enable	YNYYN	-
G5.4.2	Slow Protection	62	Hz
G5.4.3	Delay for Slow Protection (0.0 – 6550.0)	300	Second
G5.4.4	Slow 2 Protection	Disabled	Hz
G5.4.5	Delay for Slow 2 Protection (0.0 – 6550.0)	Disabled	Second
G5.4.6	Fast Protection	63.5	Hz
G5.4.7	Delay for Fast Protection (0.00-655.00)	1.0	Second
G5.4.8	Very Fast Protection	65	Hz
G5.4.9	Delay for Very Fast Protection (0.000-65.500)	0.1	Second
G5.4.10	Very Fast 2 Protection	Disabled	Hz
G5.4.11	Delay for Very Fast 2 Protection (0.000-65.500)	Disabled	Second

P-E Frequency Protection Settings



Phase Angle Jump

- 2.9.1.5 Voltage Ride-through Requirements for IBR
  - Disable anti-islanding (Comply. Set G5.3.1 Anti-islanding to Disabled)
  - Inverter shall remain on-line for a proposed positive sequence angle change < 45 degrees
    - P-E Gen 3 inverters can meet this requirement
    - However, it is suggested to MATCH the IEEE-2800 standard of 25 degree limit.
- *IEEE-1547 criteria*
- *A) Mandatory operation*
- *- Maintain the total Is above 80% of the previous value during the disturbance period. Drops for a time of less than 1 mains cycle (16 ms) are acceptable.*
  - *- Must not give a fault that stops the equipment and delays its restart.*
- *B) Momentary cessation or current blocking*
  - *- Stop energising (P = 0, Q = 0)*
  - *- Must not give a fault that stops the equipment and delays its restart.*

Inverter Backwards Compatibility

- Does the OEM believe that the current and new generators can meet the frequency ride through performance requirements proposed in NOGRR245? -->
  - The new P-E Gen. 3 inverters (i.e FS4200M/FP4200M) will meet the new NOGRR 245 requirements.
  - Until the Gen. 3 evaluation is complete, it is not known if P-E Gen.2 inverters (i.e. FS3510M and FS3350M) will meet the new requirements.
    - Cost impact is not yet determined.
  - Older inverters will require a significant cost to customers to meet backwards compatibility requirements.

P-E PSSE And PSCAD models for ERCOT

- The current set of P-E PSSE and PSCAD models can be used for simulations. New models are not required.
- TSAT report available on request

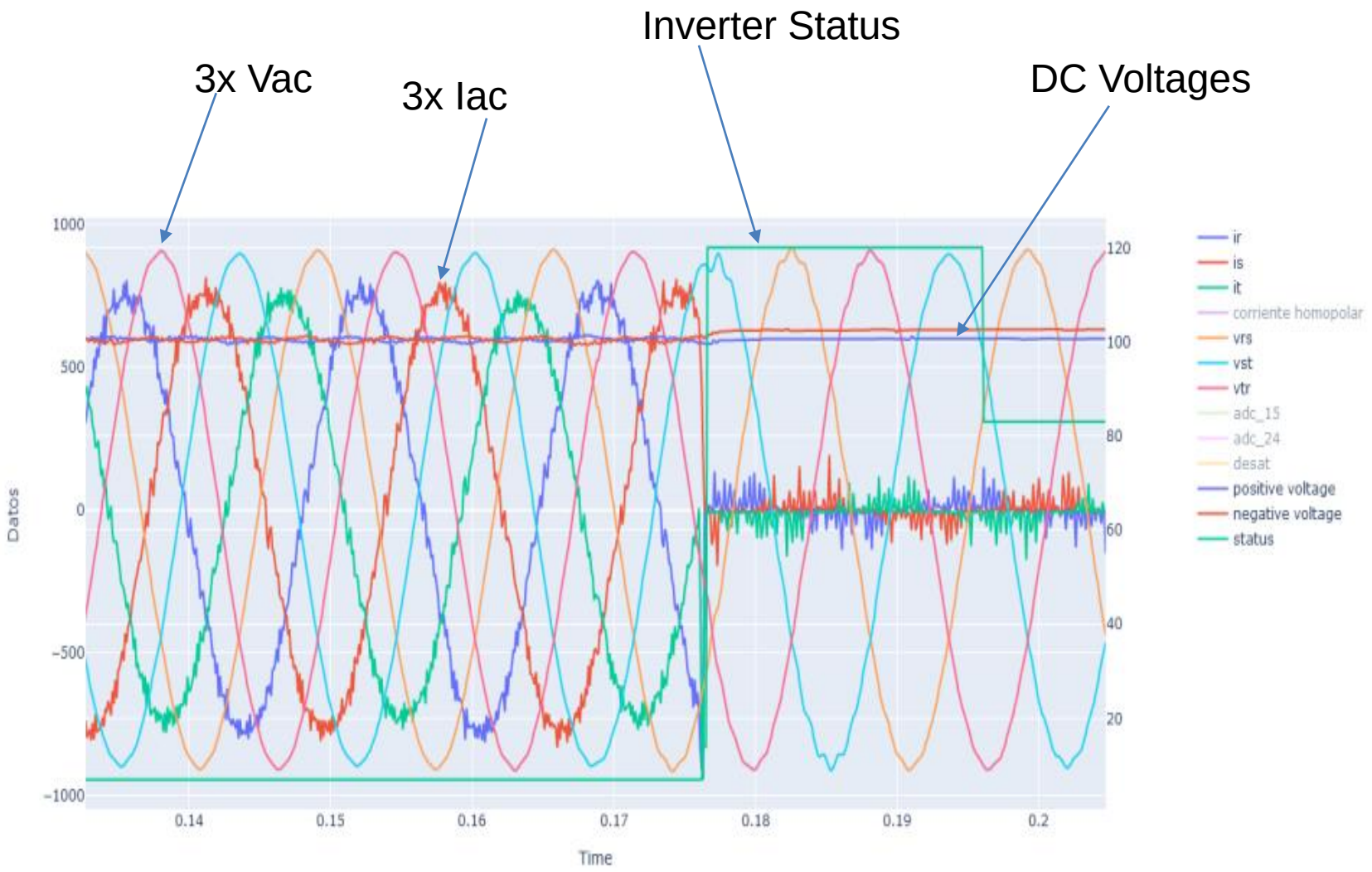
P-E Timeline

- P-E TOV Testing on new Gen.3 inverters scheduled for W14 and W15
- Unclear if existing Gen. 2 inverters already in operation will require hardware of firmware retrofits.
- IEEE-2800.2 and IEEE-2800.2 not yet released
  - IEEE-2800.1 and IEEE-2800-2 test procedures will not be available until 2024
  - Uncertainty on how to test for compliance

Data Retention

- Section 6: Disturbance Monitoring and System Protection
  - **Not applicable to individual inverters but it is important to understand what data is available.**
- Inverter parameter setting files
  - P-E is currently checking all parameters on P-E ERCOT sites to ensure the inverters are configured correctly
- P-E inverters generate an SD log with 1 second data with
  - Voltage, Current, power and Frequency
  - Inverter Status, Warning and Fault information
  - IGBT Temperature and transformer temperature information
  - Temperature and status information on individual power modules
  - Custom logs for special test monitoring
- Black box information
  - Voltage and current waveforms triggered on the last fault
  - Blackbox data is stored in the inverter for 30 days before it is overwritten
- Fast Logger files
  - Time stamped files synchronized to a GPS clock to CASIO standards

Sample Inverter Blackbox Data



Sample SD log data Analysis